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Carrier velocity in InAlN/AlN/GaN heterostructure field effect transistors on Fe-doped bulk GaN substrates

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We report microwave characteristics of field effect transistors employing InAlN/AlN/GaN heterostructures grown on low-defect-density bulk Fe-doped GaN substrates. We achieved unity current gain cutoff frequencies of 14.3 and 23.7 GHz for devices with gate lengths of 1 and 0.65 μm, respectively. Measurements as a function of applied bias allow us to estimate the average carrier velocity in the channel to be $\sim 1.0 \times 10^7$ cm/sec for a 1 μm device. Additionally, we found nearly no gate lag in the devices, which is considered a precondition for good performance under large signal operation. © *2010 American Institute of Physics*. [doi:10.1063/1.3358192]

GaN-based heterostructure field effect transistors (HFETs) have made impressive leaps in their performance over the past decade and are making inroads toward widespread commercial adoption for high frequency, high power applications.[1] Further improvements in device performance and stability can be expected as the crystal quality continues to improve.[1] Along this line, semi-insulating GaN substrates would be the ideal candidates to replace the foreign SiC substrates which are typically employed for high performance devices. The switch to a GaN substrate would be beneficial to the quality of the epitaxial HFET structure since the lattice mismatch would in principle be zero, as compared to ~3.5% for SiC substrates. However, SiC still boasts a larger thermal conductivity than bulk GaN (4.5 versus 2.3 W/cm K in undoped material) but the difference may not be large enough to favor SiC because of the adverse effect of lattice mismatch on GaN quality and heat dissipation to SiC due to low interfacial layer quality; the thermal barrier which resides at the relatively defect ridden SiC-GaN interface might negate the benefits of using the SiC substrate in the first place.[2] Since overall thermal management requires that acoustic phonons efficiently couple into the heat sink (i.e., through the substrate), such a thermal barrier is detrimental to devices on SiC but absent when using a bulk GaN substrate. On the other hand, the most important point for performance as well as reliability of these devices would be the transfer of heat out of the channel itself. Most of the heat in the channel is stored in longitudinal optical phonon modes, which cannot couple out of the channel and subsequently into the heat sink until after they have decayed into propagating longitudinal acoustic modes.[3] In this vein, arguments of one substrate over another are complicated by the fact that the heat in the channel must first be dealt with. Nevertheless, elimination of the menacing lattice mismatch induced strain, which might be the source of additional defects generated under high field and temperature operation, and improvement of the crystal quality, particularly in terms of reduced threading dislocation density and point defects garnered from using a bulk GaN wafer as the substrate[4] provide motivation to further study its use in developing high performance, reliable HFET structures.

There are few reports on GaN-based HFETs grown on bulk GaN substrates available and those exclusively utilize AlGaN barriers.[5–8] Elimination of the strain that exists in the barriers can be achieved through the use of InAlN as opposed to AlGaN barriers.[9–11] HFETs with a lattice matched InAlN barrier on bulk GaN substrates offer the promise of a completely strain-free structure. In this work we report the microwave performance of nearly lattice matched InAlN-based HFETs on bulk GaN:Fe substrates,[12] aiming to extract f_T-L_G products and average carrier velocity. In addition, we evaluated gate lag in these devices, which indicate the device ability for translating the small signal performance into large signal performance.

InAlN/AlN/GaN HFET structures were grown on c-plane semi-insulating GaN:Fe substrates (with a bulk resistivity of $\sim 10^9$ Ω cm)[4,12] by MOCVD. The HFET structures consisted of a ~2 μm thick undoped GaN layer followed by a 1 nm AlN spacer layer, an 18 nm thick $In_{0.15}Al_{0.85}N$ barrier layer, and a ~2 nm thick GaN cap layer. The structure was not passivated. We recently developed a technique to control the interface charge that can appear at the interface of the GaN:Fe substrate and the epitaxial GaN overlayer consisting of an ICP etch followed by an *in situ* H_2 etch just prior to the growth. For details on this procedure as well as growth and fabrication see Ref. 12. X-ray diffraction was used to confirm the barrier layer thickness and composition and dc performance was carried out and is reported elsewhere.[12] On-wafer microwave measurements from 2 to 20 GHz were carried out using an HP8510B vector network analyzer, and gate lag measurements were performed using a Keithley 4200 semiconductor parameter analyzer with pulse widths of 1 μsec at various quiescent bias voltages, and a duty cycle of 0.1%.

The measured S-parameters were used to compute the small signal current gain, H_{21}, which is plotted in Fig. 1 along with the maximum available gain for a device with a gate length, L_G, of 1 μm and a source-drain separation of 3 μm. The highest cutoff frequency determined is 14.3 GHz

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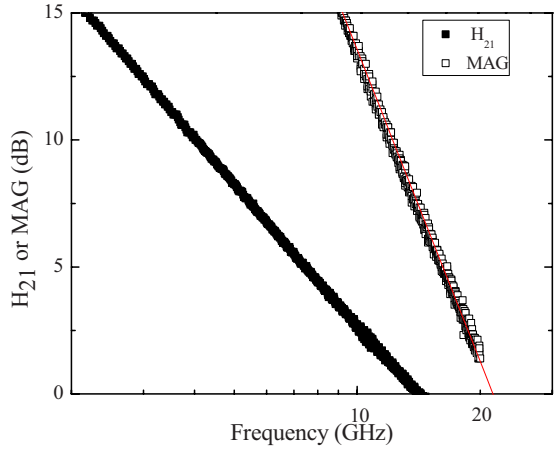

FIG. 1. (Color online) Unity current gain (solid symbols) and the maximum available gain (open symbols) for an InAlN/AlN/GaN device fabricated on a bulk semi-insulating GaN:Fe substrates with a gate length of 1 μm. f_T=14.3 GHz and f_{max}=21.5 GHz at a bias of V_D=15 V, V_G=−8 V.

near pinchoff using a drain voltage of 15 V and a gate voltage of −8 V (also achieved at a bias of V_D=10, V_G=−7).

The measured cutoff frequency is related to the total device delay time through $f_T=1/2\pi\tau_{\text{Total}}$ where τ_{Total} can be written as the sum of the intrinsic delay time, τ_{int}, the parasitic delay times associated with charging of the *RC* circuit components, τ_{RC}, and delay associated with the electron drift through the depletion region extending out from the gate on the drain side, τ_D. As the intrinsic delay time is related to the saturation velocity through $v_{\text{sat}}=L_G/\tau_{\text{int}}$, we extract the intrinsic delay time from the measured total times. This is readily achieved through the analysis proposed by Moll *et al.*[13] Measurements of the cutoff frequency at various gate and drain biases allows the analysis, as shown in Fig. 2. First, drain voltage is varied from 8 to 18 V at a constant gate voltage of −8 V and the total transit time is plotted versus the voltage drop across the channel, as shown in Fig. 2(a), i.e., $V_{\text{Channel}}=V_{DS}-I_{DS}(R_S+R_D)$, where V_{DS} is the applied drain to source voltage, I_{DS} is the drain to source current, and R_S and R_D are the source and drain resistances, respectively. Extrapolating the linear portion to zero channel voltage gives the total transit time minus that associated with drain delay, as the additional depletion region associated with the drain bias would become negligible at this bias. Using measured R_S and R_D values of 2.5 and 5 Ω, respectively, and the channel current of ~1 mA at the gate voltage of −8 V, we obtain $\tau_{\text{int}}+\tau_{RC}$=10.12 ps. Next, the gate voltage is varied at a constant drain bias (10 V) in order to generate the plot of total transit time versus inverse drain current shown in Fig. 2(b). In this case, extrapolation back to the origin can be considered to be the total transit time minus that which is associated with the charging up of parasitic *RC* components in the equivalent circuit, as the charging time associated with them would go to zero in the case of infinite current. Doing so allows us to arrive at $\tau_{\text{int}}+\tau_D$=11.12 ps. To obtain the intrinsic delay, we either solve for τ_D or τ_{RC} by subtracting $\tau_{\text{int}}+\tau_{RC}$ or $\tau_{\text{int}}+\tau_D$, respectively, from the total transit time. Using $\tau_{\text{int}}+\tau_{RC}$ we obtain τ_D=11.74−10.12 ps=1.62 ps. The intrinsic delay is therefore τ_{int}=11.12−1.62 ps=9.5 ps, which corresponds to an average carrier velocity of 1.05 $\times10^7$ cm/sec. In case we have overestimated the contribution related to the drain delay for this bias point, we can give a more conservative estimate, by using the minimum value

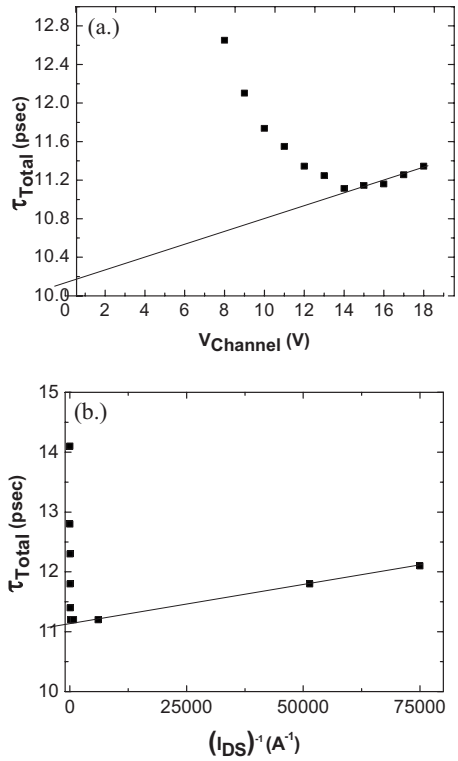

FIG. 2. Plots of total delay time: (a) vs channel voltage to extract the total time excluding drain delay (10.12 ps) and (b) vs inverse current to extract the total time excluding parasitic *RC* delay (11.12 ps). The solid lines are the extrapolation to (a) zero channel voltage and (b) infinite drain current.

of total transit time measured at V_G=−8 V [Fig. 2(a), for V_D~14 V], 11.11 ps, resulting in τ_D=11.11−10.12 ps =0.99 ps. Using this value of τ_D gives τ_{int}=11.12−0.99 ps =10.13 ps, which corresponds to an average carrier velocity of 0.99$\times10^7$ cm/sec. Reported values of electron velocity in GaN two-dimensional electron gas (2DEG) systems utilizing gated structures include 1.1$\times10^7$ cm/sec for L_G =0.29 μm,[14] 1.32$\times10^7$ cm/sec for L_G=0.15 μm,[15] 1.75 $\times10^7$ cm/sec for L_G=0.09 μm,[16] and 2.2$\times10^7$ for L_G =0.23 μm when an AlGaN/GaN/AlN barrier was employed.[17] Considering that we are using an L_G much larger than those typically used for such analysis, the extracted velocity of about 1.0$\times10^7$ cm/sec is remarkable. Clearly, shorter gate length devices should be realized. That said, preliminary results for a device with a L_G=0.65 μm yield a cutoff frequency of 23.7 GHz. This value exceeds that achieved under a similar bias condition for a similar sample grown on a sapphire substrate (15.9 GHz).[11]

We attribute the high velocity to the quality of the layer, and/or to the reduced lattice temperature expected in our layers grown on semi-insulating GaN:Fe, similar to the enhancement of electron velocity for identical devices realized on SiC as opposed to sapphire substrates.[15] Additionally, it has been recently shown using the pulsed IV measurement technique that very high velocities (3.2$\times10^7$ cm/s at a field of 180kV/cm) in our InAlN-based 2DEGs using ungated structures are attainable. This value exceeds previously reported values for velocity in ungated structures utilizing AlGaN/GaN (Ref. 19) and AlGaN/AlN/GaN (Ref. 20) of 2 $\times10^7$ and 1.1$\times10^7$, respectively. Electron velocities in high density 2DEG channels typical of GaN-based HFETs would typically be explained in terms of the hot phonon effect: Considering that the hot phonon scattering is the primary

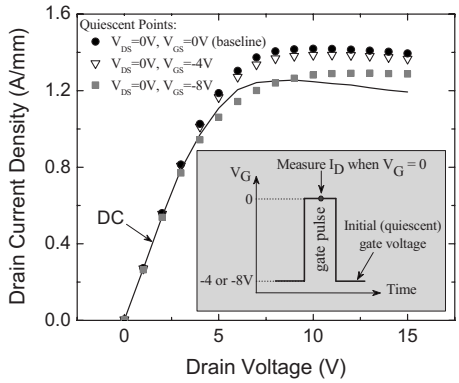

FIG. 3. Drain current measured during the V_G=0 V pulse applied to the gate (symbols) immediately after subjecting the gate to reverse biases of −4 and −8 V (near pinchoff) as a function of pulsed drain bias. Also shown are the "baseline" measurement with the gate subjected to 0 V throughout the pulsed measurement and the drain current measured under dc conditions (solid line). The inset shows a schematic of the gate pulse. The drain current is similar to the "baseline" in each of the initial reverse gate bias cases, indicating a low degree of gate lag.

detractor from carrier velocity at high fields (assuming that defect related scattering, alloy scattering, and real space transfer can be avoided), conditions at which electrons can dissipate the most power through their interaction with hot phonons should result in the highest velocities.[3] Since the amount of energy capable of being dissipated by electrons is dependant on the 2DEG density and applied power,[21] one needs to: (i) use caution when comparing measured drift velocities to ensure that the sheet densities are comparable, (ii) be cognizant of the fact that the bias condition will also affect this optimal sheet density. That said, it is unclear why yet fortuitous that the InAlN barrier channels[18] appear to exhibit higher velocities as compared to AlGaN barrier channels[20] with similar 2DEG densities.

Gate lag measurements were conducted to ascertain the feasibility of large signal operation on these layers. Typically, if gate lag is present in a device, the rf output power available would be much lower than that expected from dc output characteristics.[22] We perform the measurement in a stringent way where both the source and drain access regions are subjected to stress.[23] Fig. 3 shows the drain current density as a function of the drain voltage at dc (solid line) and under several different pulsed modes (symbols, 1-μsec pulse width, 1-msec pulse period), as well as a schematic of the timing of the pulsed measurements used to illustrate the effect of gate lag. Regarding the pulsed data, first the drain current is measured under pulsed drain voltage for V_G =0 V and is referred to as a "baseline" to determine the amount of lag. The effect of gate lag is observable by measuring the drain current under pulsed drain voltage at a gate voltage of 0 V immediately after subjecting the gate to a reverse bias, referred to quiescent point, Fig. 3. In this regard, we measure the ability of the channel to fully open up after being subjected to a moderate operation voltage (quiescent V_G=−4 V) or a nearly pinched off operation voltage (quiescent V_G=−8 V). The largest amount of lag, the percent change of drain current compared to the baseline drain current, for quiescent V_G=−8 V is 12.5% at a drain voltage of 7 V.

We demonstrated microwave performance for InAlN/AlN/GaN HFETs on semi-insulating GaN:Fe substrates. The high f_T-L_G product of 15.4 for these devices is a promising indicator for good high-frequency performance. The growth on bulk semi-insulating GaN substrates using lattice matched InAlN barrier layers as opposed to AlGaN barrier layers can yield nearly strain-free structures. This bodes well for device reliability and opens the door for operating at very high voltages in order to achieve the ultimate performance possible from GaN. Further work on passivation in order to subject devices to high voltages is warranted and further work on short L_G devices should be performed.

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