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A. Sher *College of William and Mary*

W. E. Miller *NASA-Langley Research Center*

Y. H. Tsuo *College of William and Mary*

See next page for additional authors

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Authors

A. Sher, W. E. Miller, Y. H. Tsuo, John A. Moriarty, R. K. Crouch, and B. A. Seiber

LaF₃ insulators for MIS structures

A. Sher

College of William and Mary, Williamsburg, Virginia 23185

W. E. Miller

NASA-Langley Research Center, Hampton, Virginia 23665

Y. H. **Tsuo and John A. Moriarty**

College of William and Mary, Williamsburg, Virginia 23185

R. K. **Crouch**

NASA-Langley Research Center, Hampton, Virginia 23665

8. A. Seiber

Virginia *Commonwealth University, Richmond,* Virginia 23284 (Received 8 January 1979; accepted for publication 23 February 1979)

Thin films of LaF_1 deposited on Si or GaAs substrates have been observed to form blocking contacts with very high capacitances. This results in comparatively-hysteresisfree and sharp C - *V* (capacitance-voltage) characteristics for MIS structures. Such structures have been used to study the interface states of GaAs with increased resolution and to construct improved photocapacitive infrared detectors.

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Lanthanum fluoride (LaF_3) is a fast ionic conductor with exceptional polarization properties.¹ When this material is deposited on a substrate by e-gun evaporation, the resulting film possesses thin dipole layers (\sim 50-100 Å) at its surfaces² which produce large capacitive effects. In MIS structures, the film also acts as a blocking contact for electronic conduction as long as the breakdown voltage of the device is not exceeded. The effective capacitance of the film is that of an insulating layer 100-200 Å thick with a dielectric constant of 14 (the bulk value of $LaF₃$). This capcitance is independent of the film's actual thickness as long as the measurement frequency lies below a characteristic value corresponding to the *RC* time constant of the LaF₃. For a typical 250-A. film at room temperature, we have established that the characteristic frequency is above 100 kHz. At highenough frequencies, or at low temperatures where the ionic conduction ceases, the film's capacitance is expected to decrease to its geometrical value.

We have deposited $LaF₃$ films on freshly prepared bare Si (*n* type, with a carrier concentration $n \approx 2 \times 10^{14}$ cm⁻³), on freshly prepared bare GaAs (*n* type, with $n \approx 3 \times 10^{15}$ cm⁻³), and on native-oxide-coated Si and GaAs to form composite insulators.³ The native oxide is thermally grown $SiO₂$ on the former and anodized GaAs on the latter. Back Ohmic contacts are formed for the Si samples by first e-beam depositing an Al film then sintering at 550 °C for 10 min in flowing N_2 gas, and for the GaAs samples bye-beam depositing a film of Ge-Au-Ni alloy then sintering at 450°C for 10 min in flowing forming gas. Next, the $LaF₃$ layer and a 125-Å-thick transparent Au front contact are deposited to complete the MIS structure. Finally, the sample is annealed at 400 °C in a N_2 atmosphere for 1 h.

Measured C-*V* (capacitance-voltage) characteristics are illustrated for two Si samples in Fig. 1 and for two GaAs samples in Fig. 2. No visible hysteresis is observed in the Si

FIG. 1. The C-V characteristics for two Si samples. The ramp rate for all curves is \sim 50 mV/sec.

FIG. 2. The C-V characteristics for two GaAs samples. The ramp rate for both curves is \sim 50 mV/sec.

characteristics. There is a small amount of hysteresis in the GaAs characteristics, but this is considerably less than that reported for anodized native-oxide layers alone.⁴ The GaAs devices began to leak above the largest positive voltages shown (\sim 1 V) in Fig. 2. The Si sample with a 500- \AA layer of $LaF₃$ also began to leak above 0.8 V, and the apparent onset of saturation above 0.4 Y is, in fact, due to the onset of this leakage instead.

The $C-V$ characteristic for the composite-insulatorcovered Si sample was measured at both 1 and 100 kHz, as indicated in Fig. I. In each case a saturation capacitance (the insulating-layer value) of 117 nF /cm2 and a maximum/minimum capacitance ratio of 23 was obtained. Since the theoretical capacitance of a 250- \AA layer of SiO₂ is 136 nF/cm², we infer that the 250 Å of LaF₃ contributes \sim 840 nF/cm².

Table I. Equivalent circuit parameters for GaAs MIS structures.

FIG. 3. The series capacitance C_s and dissipation factor D as a function of frequency and photon flux for the GaAs sample with a 250- \AA -thick LaF, insulator. The dots are data points and the solid curves are fits to these points determined by inserting the parameters in Table I into analytic expressions for C_x and D for the circuit shown in the inset.

This corresponds to \sim 75-Å surface dipole layers or an effective thickness for the LaF₃ film of \sim 150 Å. (In other samples, effective thicknesses of \sim 120 Å have been found.) The slight frequency dependence of the total capacitance at small bias voltages is most likely due to $Si-SiO₂$ interface-state effects,5.6 but there may also be a contribution from slow surface states in the $LaF₁$.

The $C-V$ characteristic for the composite-insulatorscovered GaAs sample in the depletion region is qualitatively similar to that of native-oxide-covered n -type GaAs.⁴ For a negative-voltage ramp, the capacitance falls below its equilibrium high-frequency value. When the ramp is reversed, the capacitance rises to its equilibrium value (reaching it at

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 $- 0.5$ V in Fig. 2) and maintains this value back to zero bias. There are a number of possible explanations for this effect. Previous workers have speculated on the existence of bulk traps⁷ or a spatially extended interface region between the GaAs and the native oxide⁴ to account for the phenomenon. Since replacing the native oxide by $LaF₃$ removes the effect, our results suggest that bulk traps are not the primary mechanism and that the proper explanation is linked to the properties of the insulating layer.

The effectively thin insulating layers permitted by the use of $LaF₃$ would seem to have many potential device applications, e.g., CCO's with lower voltages or smaller areas needed to store a given charge and more-sensitive largerdynamic-range varactors. Our direct interest in these structures, however, has been stimulated by two other types of application. The first is as an aid to the fundamental study of interface states, especially in GaAs where such states are not well characterized. The higher insulator capacitances permit higher resolution of interface-state effects in electrical measurements than otherwise possible. The second application is to improve photocapacitive MIS infrared detectors.⁸

As an illustration of the first application, we have plotted in Fig. 3 our measurements of the frequency and optical flux (Φ) variation of the total series capacitance C_s and dissipation factor *D* of the LaF₃-coated GaAs sample under zero applied bias voltage and subject to illumination on the front surface. The measured values of C_s and D are observed to be independent of the wavelength of the incident light as long as the absorption depth of the semiconductor remains within an order of magnitude of the depletion-layer thickness. The data in Fig. 3 was all taken at a wavelength of 0.820μ m. The solid lines in Fig. 3 are parameterized fits to the experimental points obtained from the equivalent circuit shown in the inset. Most of the circuit elements have a simple physical interpretation: R_0 is the sheet resistance of the front Au contact; C_0 is the insulator capacitance; C_d is the depletion-layer capacitance of the semiconductor; and C_i and R_i are the interface-state capacitance and resistance, respectively. The remaining circuit elements C_1 and R_1 represent a yet undetermined process, but probably a secondary one associated with the insulator-GaAs interface. The isolation of C_i and *R;* allows one to immediately infer the interface-state density at the Fermi level, N_i , by the relationship⁵

$$
N_i=C_i/eA,
$$

where *A* is the device area, and also the interface-state response time constant

$$
\tau_i = R_i C_i
$$

Only C_d and τ_i vary significantly with light intensity. The former increases with Φ because electron-hole pairs created by the photons absorbed in the depletion layer are separated by its large electric field, thereby decreasing its thickness. The interface-state response rate τ_i^{-1} increases linearly with $\boldsymbol{\phi},$

$$
\tau_i^{-1} = \tau_0^{-1} + K_i \Phi,
$$

because light-generated holes are driven to the interface by the depletion-layer electric field, thus providing a fast exit

mechanism for electrons localized in interface states. Numerical values of the fitted circuit parameters for both the $LaF₃$ -coated and composite-insulator-coated GaAs samples are given in Table I.

In the general case, one can identify four features of our MIS structures and measurement technique which lead to improved resolution of interface-state effects:

(i) The large values of C_0 permitted by the effectively thin insulating layers maximize the interface-semiconductor contribution to the measured electrical quantities.

(ii) The use of low-carrier-concentrations semiconductors keeps C_d relatively small, so there is less shunt effect on the C_i , R_i and C_i , R_i legs of the circuit. The carrier concentrations of our samples are significantly lower than those normally used previously.6

(iii) The measurement of C_s and D as a function of optical flux helps to identify C_i and R_i .

(iv) The comparison of the behavior of different insulators helps to distinguish different physical mechanisms, especially bulk and interface effects. To this list we could also add the temperature and bias voltage variation of C*s* and D. We expect, for instance, that such measurements will be useful in refining our understanding of the GaAs interface-state properties and ultimately providing a complete profile of the interface density of states.

In our second application, photocapacitive MIS infrared detectors⁸ that operate at room temperature have been built from both LaF_3 -covered and composite-insulatorcovered Si and GaAs. These new detectors have unoptimized detectivities at 13 Hz of \sim 2 \times 10¹³ W⁻¹ cm Hz^{1/2} for Si and $\sim 1 \times 10^{13}$ W⁻¹ cm Hz^{1/2} for GaAs. The former number represents an order-of-magnitude improvement over both our initial Si devices,⁸ which used $SiO₂$ insulating layers, and conventional photovoltaic Si detectors.⁹ Additional details on this application will also be presented elsewhere.

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