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Growth and characterization of SiC epitaxial layers on Si- and C-face 4*H* SiC substrates by chemical-vapor deposition

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High-quality Schottky junctions have been fabricated on *n*-type 4*H* SiC epitaxial layers grown by chemical-vapor deposition on C- and Si-face substrates in order to understand the effect of growth direction on the growth mechanism and formation of defects. Atomic force microscopy analysis showed dramatic differences between the surfaces of SiC epilayers grown on C and Si faces. There was a significant step bunching in the SiC grown on Si-face substrates. Current-voltage, capacitance-voltage, and deep-level transient spectroscopy (DLTS) measurements were carried out on the Schottky junctions to analyze the junction characteristics. The Schottky junctions on C-face SiC showed larger barrier heights than those on Si-face SiC, showing that each face has a different surface energy. The barrier heights of Ni Schottky junctions were found to be 1.97 and 1.54 eV for C-face and Si-face materials, respectively. However, the deep-level spectra obtained by DLTS were similar, regardless of the increased surface roughness of the Si-face 4*H* SiC. © *2005 American Institute of Physics*. [DOI: 10.1063/1.2132520]

Recently, research has shifted to 4*H* SiC from 6*H* SiC due to its higher electron mobility with smaller anisotropy and relatively lower dopant ionization energies. 4*H* SiC also shows desirable features such as a wide band gap, high thermal conductivity, high breakdown field, and high-power device applications at high temperatures and high frequencies.[1–4] Schottky diodes made on 4*H* SiC are highly useful in high-power rectifiers because of the high voltage (400–1100 V), low on-state voltage drop, low leakage current, and fast switching speed.[5] Since there is a surface energy difference between $(000\bar{1})$ C-face and (0001) Si-face substrates,[6] there should be a difference in the electrical properties of devices made on these faces. Interface reaction is more active on the C face than on the Si face; therefore the interface state density is higher on C-face SiC. A similar kind of properties is also noticed on the Schottky junctions for N- and Ga-polarity GaN layers due to surface reconstruction.[7]

To prepare unintentionally doped SiC epitaxial layers, Si- and C-face 4*H* substrates ($n \sim 10^{18}$ cm^{-3}) obtained from the Cree Research, Inc. were cleaned sequentially in acetone, xylene, and methanol using an ultrasonic bath, then cleaned with a Caro etch, rinsed in distilled water, and finally flushed with N_2. The SiC epitaxial layers were deposited on cleaned *n*-type off-axis 4*H*-SiC substrates, inclined 8° toward $[11\bar{2}0]$ in order to avoid the formation of rough and mosaic patterns on the epitaxial layers. The C- and Si-face substrates were etched under H_2 flow rates of 6 l/min at 1400 °C, not only to remove surface scratches incurred while polishing the substrates, but also to form a stepped pattern. 2% SiH_4 and 2% C_3H_8 in H_2 were used as source gases for Si and C, respectively. High-purity industrial-grade H_2 was used as a carrier gas and reductant for the growth of epitaxial layers. 2% N_2 in H_2 was used for nitrogen doping in the epilayers. To deposit epilayers, the substrate temperature and the reactor pressure were kept at 1550 °C and 80 Torr, respectively. A C/Si ratio of 1.0 was maintained in the gas phase. The nucleation growth rate is higher on C-face substrates than on Si-face substrates.

The Schottky junctions were fabricated on 5-μm-thick Si- and C-face SiC epitaxial layers employing a shadow

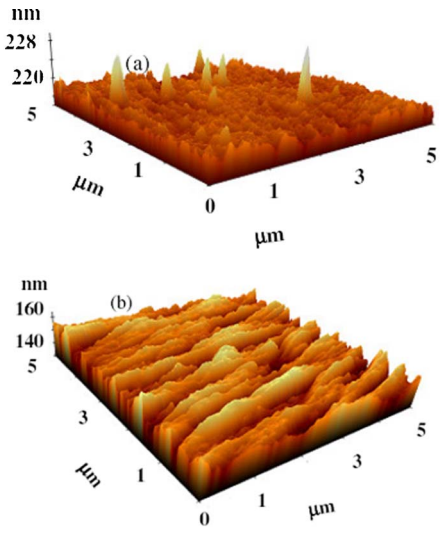

FIG. 1. (Color online) AFM images of SiC epilayers grown with C/Si=1 on (a) C-face and (b) Si-face 4*H* SiC substrates by CVD.

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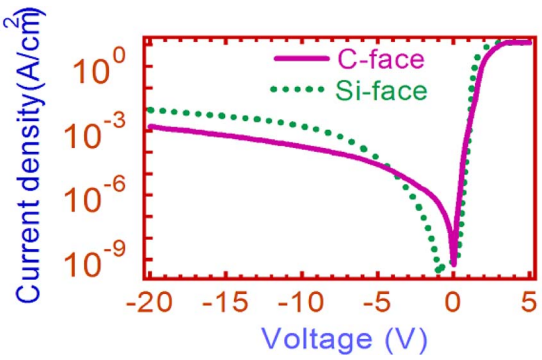

FIG. 2. (Color online) *I-V* curves of Schottky junctions with 1 mm diameter fabricated on C-face and Si-face 4H SiC epilayers.

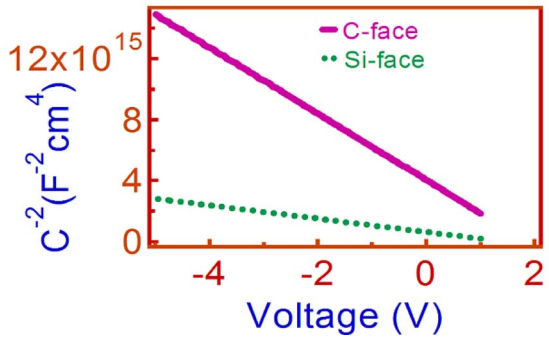

FIG. 3. (Color online) A plot of $1/C^2$ vs V for Schottky junctions with 1 mm diameter fabricated on C-face and Si-face 4*H* SiC epilayers.

mask with diameters of 0.5, 1.0, and 1.5 mm. On the back sides of the SiC substrates, Ti (200 Å)/Ni(800 Å)/Al (100 Å) metals were deposited by electron beam evaporation and then annealed at 1000 °C for 5 min in Ar to form Ohmic contacts for current-voltage (*I-V*), capacitance-voltage (*C-V*), and deep-level transient spectroscopy (DLTS) measurements. Ni (300 Å)/Au (500 Å) metals were deposited on the surfaces of Si- and C-face epitaxial layers as Schottky junctions. The rectifying properties of the Schottky contacts were improved by annealing the samples at 500 °C for 15–20 min in an Ar atmosphere. The surfaces of the grown layers were studied using an atomic force microscope (AFM). The *I-V* measurements were done using an HP4145 parameter analyzer, and *C-V* measurements were carried out using an HP4284A LCR meter in the 1 k–1 MHz frequency range. A DLTS system with a liquid nitrogen cryostat was used to characterize the defect levels in the temperature range from 70 to 700 K. For these experimental studies, 40 diodes with three different diameters of 0.5, 1.0, and 1.5 mm on each 1.1×1.1 cm^2 substrate were used, and 25–30 data points were averaged. In order to obtain reproducibility, we have fabricated several samples and several runs using the chemical-vapor deposition (CVD) system. The mapping studies on each sample are under investigation.

The AFM analysis revealed that the SiC epilayer grown on a C face contained small and large nano-tube like structures, as shown in Fig. 1(a). The epilayers on Si faces showed large step heights, from step bunching, which are 20–30 times the unit-cell height (10.08 Å) of 4*H* SiC [Fig. 1(b)]. In general it has been reported in literature that the heights are one or two times the bilayer of 4*H* SiC.[8] In the present case the larger heights could be due to the combination of multiple step heights. It is evident from the AFM analysis that the Si-face epilayer showed greater surface roughness than the C-face epilayer.

The diode current-voltage relationship governed by the thermionic emission theory is expressed as[9]

$$I = I_0 e^{q(V-IR_s)/\eta kT}[1 - e^{-q(V-IR_s)/kT}], \quad I_0 = A^* T^2 e^{-q\phi_b/kT}, \tag{1}$$

where V is the applied bias, I is the measured current, I_0 is the saturation current, R_s is the specific on-resistance, η is the ideality factor, k is the Boltzmann constant, T is the temperature, and ϕ_b is the barrier height. The leakage currents of C- and Si-face Schottky junctions were found to be 10^{-3} and 10^{-2} A/cm^2 at −20 V, respectively, as shown in Fig. 2. By simulating experimental results, the specific on-resistance was found to be 0.12 Ω cm^2 for the Si face and 0.3 Ω cm^2 for the C face. From the *I-V* data, there is a little difference in current transport properties between SiC grown on the C or Si face.

The barrier height was calculated from the *C-V* measurements using the conventional plot of I/C^2 vs V, as shown in Fig. 3, using the relations[9,10]

$$\phi_b = V_{\rm bi} + \frac{kT}{q}\ln\left(\frac{N_C}{N_D}\right) + \frac{kT}{q} - \Delta\phi, \quad \Delta\phi = \sqrt{qE_m/4\pi\varepsilon_s}, \tag{2}$$

$$E_m = qN_C\alpha/\varepsilon_s + qN_D(\alpha - w)/\varepsilon_s, \quad w = \sqrt{2\varepsilon_s V_{\rm bi}/qN_D}, \tag{3}$$

$$N_D = \frac{2}{q\varepsilon_s\{-[d(1/C^2)/dV]\}A^2}, \tag{4}$$

where $V_{\rm bi}$ is the built-in potential, N_D is the donor concentration, N_C is the effective density of states in the conduction band, $\Delta\phi$ is the image force lowering of the barrier, E_m is the maximum electric field, ε_s is the dielectric constant of the semiconductor, α is the distance of heavily doped region extension, w is the depletion width, and A is the area of the diode. The physical parameters of the C- and Si-face Schottky junctions obtained from the *C-V* measurements are shown in Table I. The carrier concentration was found to be 3.3×10^{16}/cm^3 for the Si face and 6.6×10^{15}/cm^3 for the C face.

TABLE I. Physical parameters of C- and Si-face Schottky junctions.

Face	ϕ_b (V)	$V_{\rm bi}$ (V)	$E_m(10^5$ V/cm)	$W(\mu$m)	$\Delta\phi$ (V)	N_D(cm^{-3})
C	1.97	1.86	8.5	0.555	0.107	6.6×10^{15}
Si	1.54	1.47	7.8	0.221	0.106	3.3×10^{16}

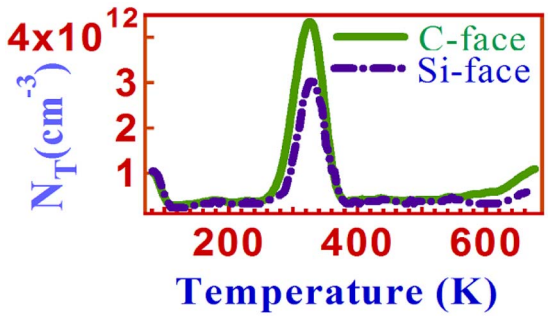

FIG. 4. (Color online) Deep-level transient spectra for the traps in SiC epilayers grown on C- and Si-face 4*H* SiC substrates.

The DLTS spectrum shown in Fig. 4 is dominated by traps at <100 K due to Ti, and the Z_1/Z_2 trap at 330 K, which has been proposed to be related to the silicon antisite (Si_C) or carbon vacancy (V_C).[11,12] Experimental work (Ref. 12) shows that increasing the carbon decreases the height of this peak, suggesting that the defect may be due to Si_C or V_C. However, theoretical estimates for the formation energy, negative-*U* nature, and acceptor nature may conflict with this assignment.[13] Overall, there is a negligible difference between the deep-level spectrum in 4*H* SiC grown on the carbon or the silicon face.

The Arrhenius plot is shown in Fig. 5. The activation energy levels and capture cross sections were found to be $E_c-0.14$ and $E_c-0.63$ eV, and 7×10^{-15} and 9×10^{-15} cm^2 for Ti and Z_1/Z_2, respectively. There was also a trap at 0.64 eV, with a larger capture cross section of 4×10^{-14} cm^2 superimposed on the peak at 330 K. This second trap at 330 K appeared in higher concentration in the SiC grown on the C face, with a 0.63:0.64 eV trap ratio between 2.5:1 and 2.7:1, and was barely detectable in the 4*H* SiC grown on the Si face. If both traps (0.63 and 0.64 eV) were due to the Z_1 and Z_2 levels, respectively, their concentrations would be expected to be the same, assuming identical formation energies on hexagonal and cubic lattice sites and identical densities of possible sites. The observation that they are not always present in a one-to-one ratio suggests that the traps comprising this peak are the Z_1/Z_2 trap at 0.63 eV and some other trap at 0.64 eV. There have been other reports of overlapping

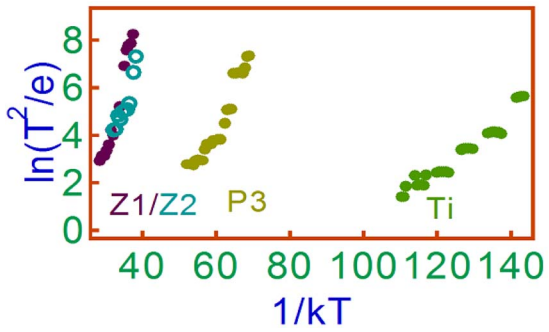

FIG. 5. (Color online) Arrhenius plot for the traps in 4*H* SiC grown on the C and Si face. The traps were present in both sample types, although in slightly different proportions.

peaks in this region, with differing annealing temperatures of 600, 1200, 1400, and over 1700 °C.[13–16] The different annealing temperatures indicate a variety of compositions. The trap at 0.3 eV was present in both samples. It is similar in character to the P_3 trap described in Ref. 14, although the concentration we measured is three orders of magnitude lower.

C/Si ratios outside of the windows of 2–6 for growth on the Si face and 2–3 for growth on the C face reportedly result in nonspecular growth.[6] From the AFM images of the growth with C/Si ratio of 1, the surface with greater roughness was that of the Si face. Aside from the whiskers, growth on the C face is specular. From the difference in surface morphologies, one would expect that the defect structure might be different for the C- and Si-face SiC. However, the fact that the DLTS spectra were nearly identical indicates that formation of the macrosteps during growth on the Si face does not result in additional electrically active defects. 4*H* SiC has also been characterized for C/Si ratio of 2 on both C and Si faces, with no differences seen in either photoluminescence or DLTS in literature.[17]

In summary, the AFM analysis distinguished a difference between the surface roughness of SiC epitaxial growth on C-face and Si-face 4*H* substrates. The Schottky junctions fabricated on C-face SiC epilayers showed a lower leakage current, as compared with that of Si-face epilayers. The traps Ti and *Z*1/*Z*2 with more or less the same concentrations were observed in C-face and Si-face Schottky junctions.

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