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Bias dependent two-channel conduction in InAlN/AlN/GaN structures

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Due to growth temperature differences during deposition of GaN heterostructures utilizing InAlN barriers, an inadvertent parasitic GaN layer can form in the InAlN barrier layer. In structures utilizing AlN spacer layers, this parasitic layer acts as a second conduction channel with a carrier density dependent upon polarization charges and lattice strain as well as the surface potential. The effect of an additional GaN spacer layer in InAlN/AlN/GaN structures is assessed using simulations, electron-microscopy observations, magnetoconductivity measurements with gated Hall bar samples, and with quantitative mobility spectrum analysis. We propose a possible formation mechanism for the parasitic layer, and note that although the additional unintended layer may have beneficial aspects, we discuss a strategy to prevent its occurrence. © *2010 American Institute of Physics*. [doi:10.1063/1.3330627]

I. INTRODUCTION

InAlN-based heterostructure field effect transistors (HFETs) have gained much attention in recent years due to their promise to deliver high current and high power densities in devices that are strain free due to the lattice matching between GaN and InAlN when the In composition is near 17%.[1] Recent advances in the growth of InAlN have resulted in respectable HFET performance in devices employing this lattice matched barrier.[2–5] Reported performance metrics include current densities for forward biased gates of up to 2.3 and 2.8 A/mm under dc and pulsed bias, respectively,[1] extrinsic transconductance of 675 mS/mm for barrier thicknesses scaled down to 3 nm without a reduction in 2DEG density,[3] a cutoff frequency-gate length (f_T-L_G) product of 15.4,[4] and operation at temperatures up to 1000 °C.[1] These results support the promise of this materials system for HFETs pending the resolution of some further technological and materials challenges. In this regard, we describe here and discuss the impact of an inadvertent GaN layer that can form between the intentional AlN spacer layer and the InAlN barrier layer.[6]

II. EXPERIMENT

The InAlN-based HFETs were grown on sapphire substrates in a low-pressure custom-designed organometallic-vapor-phase epitaxy system. Trimethylgallium, trimethylaluminum, trimethylindium, and ammonia were used as the Ga, Al, In, and N sources, respectively. An initiation layer of AlN (250 nm) was grown at ~1030 °C at a chamber pressure of 30 torr, followed by 3.0 μm of undoped GaN deposited at ~1000 °C at 200 torr. Next, an optimized AlN spacer layer was grown at 1000 °C with a thickness of 0.8–1 nm, which was determined from x-ray diffraction data using a superlattice calibration structure grown under identical conditions. Next, the temperature was ramped down to 740 °C and the carrier gas switched from H_2 to N_2 for ~15 nm of InAlN growth. The structure was capped with 1–2 nm of GaN. The gated Hall bars were fabricated using Ti/Al/Ni/Au Ohmic contacts followed by etched mesa isolation in a SAMCO inductively coupled plasma etch tool using a Cl-based chemistry. The Pt/Au (30/50 nm) gate was fabricated using a standard liftoff procedure.

III. RESULTS AND DISCUSSION

The inadvertent GaN layer can be observed in conventional transmission electron microscope (TEM) and is particularly evident in high-angle annular-dark-field (HAADF) scanning TEM (STEM) images of the HFET structure, as shown in Figs. 1(a) and 1(b), respectively. The bright-field image (a) reveals the presence of a ~2-nm-thick darker contrast region just above the light contrast AlN layer, whereas the HAADF STEM image (b) shows the characteristic lighter contrast associated with a higher atomic weight material. As revealed by the energy dispersive x-ray spectroscopy (EDSX) line profile in Fig. 1(c), this region unexpectedly contains a considerable quantity of gallium.

An inadvertent layer of GaN in such a location would constitute a quantum well since the conduction band minimum of GaN is much lower than the neighboring AlN spacer and InAlN barrier layers. The effect of such an additional quantum well would be to effectively partition the electrons that would normally have filled the intentional triangular quantum well at the AlN/GaN (lower) interface. The percentage of electrons residing in the unintentional well would depend critically on its thickness, the spontaneous polarizations of the constituent materials, the strain state of the system, and the gate voltage (V_G). Table I shows ATLAS simulation

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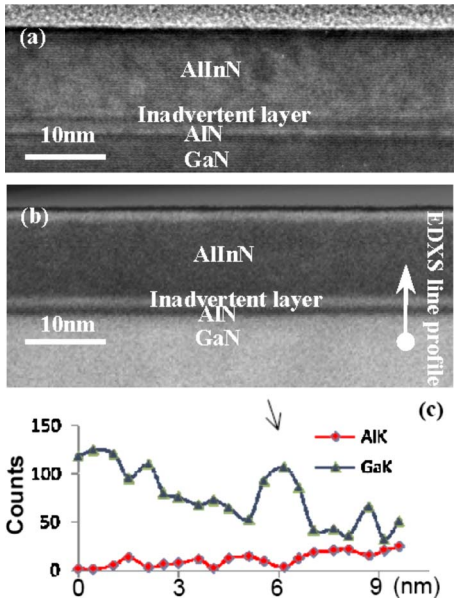

FIG. 1. (Color online) (a) Bright-field TEM image, (b) HAADF STEM image, and (c) corresponding EDXS line profile of the InAlN/AlN/GaN region illustrating inclusion of the inadvertent Ga interlayer. The EDXS line profile demonstrates that the inadvertent layer contains considerable Ga.

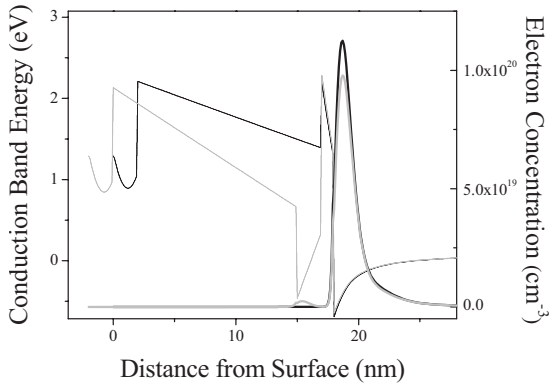

FIG. 2. Calculated band diagrams (dotted lines) and electron concentrations (solid lines) at zero gate bias for the InAlN/AlN/GaN HFET structure with no unintentional GaN interlayer (black) and with a 2 nm GaN interlayer between the AlN spacer and the InAlN barrier layer (gray). The plot for the structure, which includes the 2 nm GaN layer is shifted in such a way as to make the intentional triangular well at the AlN/GaN interface overlap.

results for the density of electrons in the intentional and unintentional quantum wells for various thicknesses of the unintentional interlayer at zero bias and assuming a Pt gate (with a work function of 5.6 eV). The spontaneous polarization values taken from Ref. 7 are 5.62×10^{13}, 2.12×10^{13}, and 4.61×10^{13} e^-/cm for the AlN, GaN, and $In_{0.15}Al_{0.85}N$, respectively. Taking the AlN spacer layer to be fully strained induces an additional piezoelectric polarization of 2.90×10^{13} e^-/cm. The InAlN layer's polarization is assumed to have a bowing parameter of -4.37×10^{13} e^-/cm, and the composition of 15% In was used, which is closer to being lattice matched than the typically reported lattice matched composition of 17% for our (compressively strained) GaN on sapphire films.[8] The total concentration of electrons in the system slightly decreases while the fraction of electrons in the unintentional layer increases with the thickness of the unintentional well, as shown in Table I. Moreover, any strain relaxation in the AlN spacer layer would reduce the polarization's piezoelectric component and tend to decrease the electric field in the inadvertent well, thereby increasing itscarrier density. The unintentional GaN channel begins to fill appreciably with electrons for thicknesses ~1–2 nm. The calculated conduction band edge and electron concentrations are shown in Fig. 2 for the cases with no interlayer and a 2 nm unintentional interlayer.

To delineate the impact of the inadvertent layer on conductivity, we performed longitudinal magnetoresistance and Hall measurements at magnetic fields up to 6.9 T on a gated Hall bar structure at 4.2 K. For gate voltages smaller than −1.5 V, we observe well-pronounced Shubnikov–de Haas (SdH) oscillations as shown in Fig. 3(a). This is consistent with full depletion of the parasitic channel so that only the primary (intentional) 2DEG layer is present. At higher V_G (toward zero bias), the magnitude of the SdH oscillations decreases with bias while their period remains fixed, which appears to correlate with onset of the parasitic channel located between the 2DEG and the top gate. We could not resolve SdH oscillations for gate biases greater than −1 V, where the population of electrons in the unintentional GaN layer is no longer negligible. The carrier density extracted from the period of the SdH oscillations (1.34×10^{13} cm^{-2} at $V_G=-2$ V) agrees well with that obtained from the Hall measurements.

Figure 3(b) plots carrier densities (filled points) and mobilities (open points) derived from the Hall and magnetoresistivity measurements at each gate voltage. The squares in this figure are taken from the "raw" magnetotransport data

TABLE I. Calculated 2DEG density in the intentional and unintentional quantum wells as a function of the unintentional GaN interlayer thickness. The values in brackets represent the same assuming that the AlN is partially relaxed (20%). The electron population in the unintentional layer quickly increases when the AlN spacer layer relaxes.

Thickness of GaN interlayer (nm)	0	1	2	3	4
Intentional 2DEG [with 20% relaxed AlN] ($\times10^{13}$)	2.45 [2.41]	2.24 [2.21]	2.12 [1.99]	1.74 [1.61]	1.46 [1.35]
Unintentional [with 20% relaxed AlN] ($\times10^{13}$)	⋯	0.0 [0.0]	0.03 [0.15]	0.40 [0.53]	0.68 [0.79]
% in unintentional	⋯	0% [0%]	1.4% [7.0%]	18.7% [24.8%]	31.8% [36.9%]

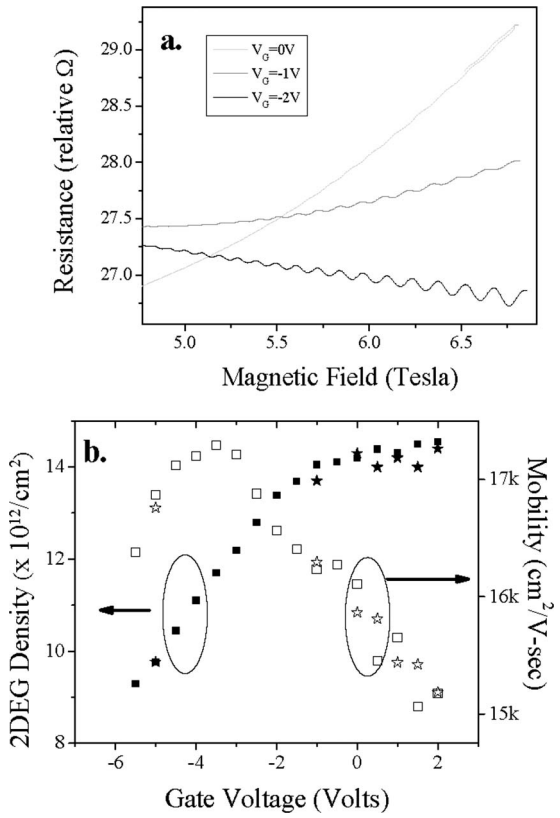

FIG. 3. (a) SbH oscillations for gate biases of −2, −1, and 0 V (the 0 V curve is offset for clarity). The oscillations are strongest when the parasitic channel is depleted at large negative biases, become weaker for −1 V with the onset of parasitic conduction, and are barely discernable at all for 0 V where the parasitic channel is more heavily populated. (b) Carrier density (solid points) and mobility (open points) for the InAlN barrier HFET structure shown in Fig. 1, as determined from gated Hall bar measurements. The squares are "raw" data (assuming no mixed conduction), while the stars are the intentional 2DEG layer's density and mobility as extracted from the QMSA.

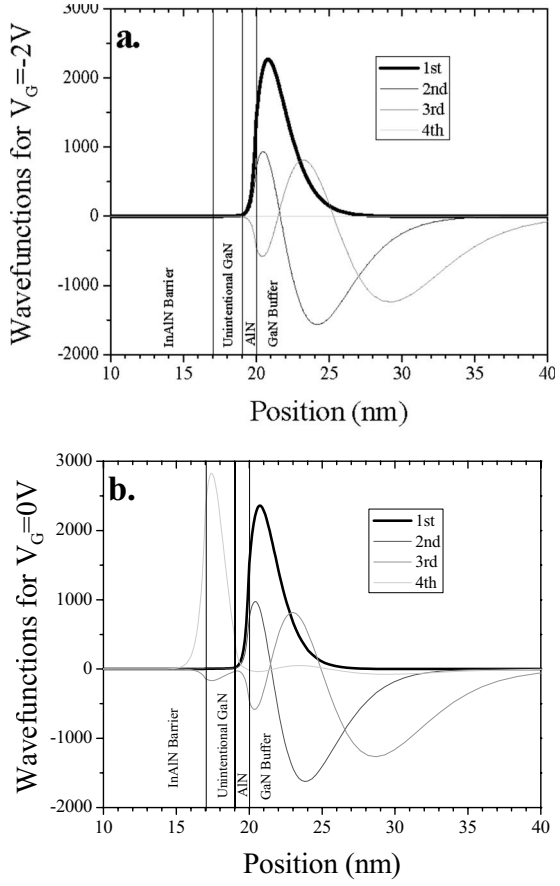

FIG. 4. Wave functions for the InAlN/GaN/AlN/GaN heterostructure with a 2 nm GaN interlayer at applied gate biases of (a) −2 and (b) 0 V. There is very little overlap between the wave functions associated with the two channels, therefore, one would not expect the high electron mobility associated with the intentional 2DEG to be degraded appreciably when the second channel is populated.

assuming a single electron species. However, mixed conduction effects are expected to arise at gate biases for which the unintentional parasitic channel becomes populated. To quantify this contribution, we treated the same magnetic-field-dependent Hall and resistivity data with the quantitative mobility spectrum analysis (QMSA),[9] which is able to delineate multiple conduction channels having differing mobilities. The stars in Fig. 3(b) display the resulting QMSA densities and mobilities for the primary 2DEG channel at various gate biases, which are seen to be effectively unchanged from the "raw" results represented by the squares.

QMSA additionally determines that for zero and positive gate biases but not $V_G \leq -1$ V, a second electron species with very low mobility contributes in parallel to the primary high-mobility carrier. This finding is consistent with the bias-dependent SdH data, and also with the simulation discussed above, if the lower-mobility species is associated with electrons residing in the unintentional GaN interlayer. Since the mobility of the second population is quite low in relation to the maximum available magnetic field strength of 6.9 T (i.e., $\mu B_{\max} \ll 1$), QMSA cannot reliably extract its density and mobility separately but only the net conductivity corresponding to the density-mobility product. This additional conductivity contribution is found to increase by a factor of ~6 as the gate bias increases from 0 to 2 V. If we further take the parasitic channel's carrier density at zero bias to be 1.4% of the total, as calculated by the simulation summarized in Table I for a 2-nm-wide interlayer, QMSA derives a mobility of 403 cm^2/V s for that layer. Performing the same analysis with a channel width of 3 nm (22.2% of the carriers in the interlayer) implies a corresponding mobility of 30 cm^2/V s. Such a low mobility in this range is expected inside the unintentional well, due to the large alloy potential of InAlN (compared to AlGaN)[10] and the large subsequent alloy scattering.[11,12] Typical Hall measurements would not capture the contribution by carriers populating the unintentional layer due to their very low conductivity (at most 0.25% of the total).

Despite the nearby presence of the parasitic layer, we expect the intentional channel to maintain its high mobility because its electron wave functions do not extend into the lower-quality region. Figure 4 illustrates simulated wave function distributions for the structure with a 2 nm unintentional GaN interlayer at V_G=−2 and 0 V. Under reverse bias, none of the four lowest energy levels reside in the parasitic channel, hence it is unpopulated. At zero bias, the fourth-lowest level and part of the third resides in the unintended layer, although each wave function more or less resides in

one layer or the other with negligible overlap. Furthermore, the enhanced screening from alloy scattering afforded by the additional GaN spacer layer may actually *improve* the overall mobility as previously demonstrated for an AlGaN/GaN/AlN/GaN structure.[13]

We believe that the unintentional interlayer forms as a result of GaN being deposited on the sample holder during growth of the GaN buffer layer (3-μm-thick). After the AlN spacer layer is grown, we ramp down the temperature to 740 °C and switch the carrier gas from H_2 to N_2. During this time (6.5 min), GaN deposited on the holder may migrate and be deposited onto the sample surface. Such a mechanism seems plausible considering the abruptness of the unintentional GaN interlayer's interfaces, as shown in Fig. 1. In order to test this possibility, we grew another structure wherein the growth was interrupted prior to the deposition of the spacer and barrier layers. The sample holder was then replaced with a clean (GaN free) one, and subsequently the growth was resumed with a 100 nm thick GaN followed by the AlN spacer, AlInN barrier, and GaN cap layers. The subsequent TEM analysis demonstrated that the unintentional GaN interlayer in this epilayer was much thinner (~1 nm) than the interlayer unintentionally deposited when the growth was not interrupted. Of course, these findings also imply that there may be unintentional Ga being incorporated in all layers (i.e., the AlN and InAlN layers).

IV. SUMMARY

In conclusion, gated Hall bar measurements and QMSA were performed on InAlN barrier HFET structures known to have unintentional GaN interlayers between the AlN spacer and the InAlN barrier. We showed that such a barrier will become populated with electrons as the layer becomes thicker, and that despite the low mobility in the GaN interlayer channel, the mobility in the intentional 2DEG remains high. We do not intend to imply that all previous reports on InAlN/GaN heterostructures suffered from the inclusion of an inadvertent GaN layer but suggest that an inadvertent layer could be a source of discrepancy in heterostructures wherein the 2DEG density is unexpectedly low,[11] and also point out that the HAADF TEM images tend to illustrate the inadvertent layer more clearly than conventional bright-field images. We propose that the unintentional interlayer is deposited during the hold time while the system is ramping down in temperature and changing its background carrier gas, and that the source of Ga is related to the hot sample holder. This is supported by the fact that the thickness of the GaN interlayer decreased when the growth was interrupted and a clean sample holder used for the final HFET structure growth.

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