2013

Ultra-low-energy non-volatile straintronic computing using single multiferroic composites

Kuntal Roy
Virginia Commonwealth University, royk@vcu.edu

Roy, K. Ultra-low-energy non-volatile straintronic computing using single multiferroic composites. Applied Physics Letters, 103, 173110 (2013).

Ultra-low-energy non-volatile straintronic computing using single multiferroic composites

Kuntal Roy[a),b)]
School of Electrical and Computer Engineering, Virginia Commonwealth University, Richmond, Virginia 23284, USA

(Received 24 August 2013; accepted 9 October 2013; published online 23 October 2013)

The primary impediment to continued downscaling of traditional charge-based electronic devices in accordance with Moore's law is the excessive energy dissipation that takes place in the device during switching of bits. One very promising solution is to utilize multiferroic heterostructures, comprised of a single-domain magnetostrictive nanomagnet strain-coupled to a piezoelectric layer, in which the magnetization can be switched between its two stable states while dissipating minuscule amount of energy. However, no efficient and viable means of computing is proposed so far. Here we show that such single multiferroic composites can act as universal logic gates for computing purposes, which we demonstrate by solving the stochastic Landau-Lifshitz-Gilbert equation of magnetization dynamics in the presence of room-temperature thermal fluctuations. The proposed concept can overwhelmingly simplify the design of large-scale circuits and portend a highly dense yet an ultra-low-energy computing paradigm for our future information processing systems. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4826688]

Utilizing electron's spin rather than its charge as state variable has been widely studied in the field of so-called spintronics,[1] particularly in the context of nanomagnets,[2,3] since it can potentially lead to ultra-low-energy computing. Recently, it has been shown that the magnetization of a 2-phase multiferroic composites,[4] comprised of a single-domain magnetostrictive nanomagnet strain-coupled to a piezoelectric layer, can be switched between its two stable states with a tiny voltage of few tens of millivolts at room-temperature.[5–7] Such electric-field induced magnetization switching mechanism dissipates a miniscule amount of energy of only ~1 attoJoule (aJ) with sub-nanosecond switching delay at room-temperature[6] and thus it can potentially extend the lifeline of conventional electronics.[8–10] Experimental efforts to demonstrate the operation of such straintronic devices are emerging too.[11–14]

Here, we propose a viable and an efficient way of devising logic elements exploiting such devices for general-purpose computing. With experimentally feasible parameters, we theoretically demonstrate that such single multiferroic elements can act as universal logic gates. Traditionally, implementing logic gates according to magnetic quantum cellular automata (MQCA) architecture[7,15–17] takes multiple elements to implement the same logic functionality and thus incurs more complexity, switching delay, energy dissipation, and area on a chip. Therefore, the proposed concept has profound promise in simplifying the design of large scale circuits and consequently improving the performance metrics drastically.

Although a number of proposals have been reported on spintronics for the purposes of computing,[20–24] the present proposal with single multiferroic composite structures is unique in the sense that it simultaneously satisfies the following important attributes of general-purpose computing: ultra-low-energy dissipation, fast (sub-nanosecond) switching, room-temperature operation, and highly dense logical functionality per unit area. Using single multiferroic elements as universal logic gates while simultaneously being highly energy-efficient would facilitate to cram more functionality on a chip and hence it has immense potential to be an important contributor to Beyond Moore's law technologies.[8,10]

The basic structure of the proposed universal logic gates using single multiferroic elements is shown in Fig. 1. Application of voltages at the input terminals *A* and *B* generates strain in the piezoelectric layer (two inputs generate *twice* as much strain compared to when voltage is applied to only one input) and the strain is transferred elastically to the magnetostrictive nanomagnet (M1 layer).[5] This generates a stress-anisotropy that can overcome the shape-anisotropy of the nanomagnet M1 to switch its magnetization (LOGIC operation, to be described later).[5,25] The magnetization direction of the M1 layer can be switched opposite to that of the M2 layer (with fixed magnetization direction) by application of a voltage at the *Set* terminal on the piezoelectric layer. This is termed as SET operation, which is required to perform before a LOGIC write operation, however, once the bit is written, the logic output can be read (READ operation) as many times as required before any further write operation. The output of the gate (the Out terminal) is extracted from the read-line measuring magnetoresistance (MR),[18,19] of the structure, i.e., if the relative orientation of the magnetizations in the layers M1 and M2 is parallel, MR is *low*, and the output is *logic 0*, while for the anti-parallel case, MR is *high* and the output is *logic 1*. Since the output from a gate is connected to the inputs of the gates on the next stage and the inputs are on a *thick* piezoelectric layer (so it does not load the output much), the universal logic gates can be concatenated to achieve any Boolean logic function.

[a)]Electronic mail: royk@vcu.edu.
[b)]Present address: School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907, USA

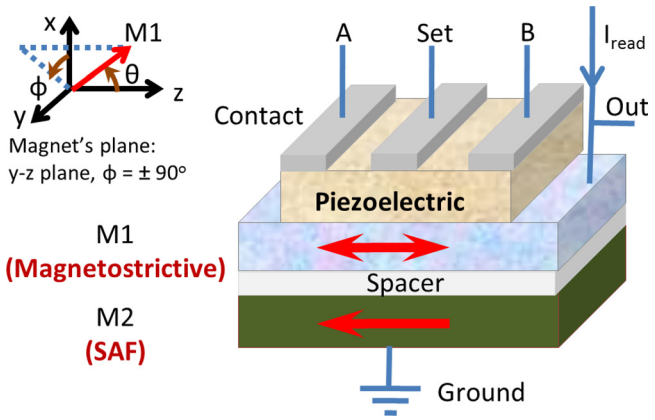

FIG. 1. Schematics of the proposed single-element straintronic universal logic gates. By applying voltages at the terminals A and B, the magnetization of the magnetostrictive nanomagnet (layer M1) can be switched. The *spacer* layer is a thin layer ($\sim$1 nanometer) made of materials like Magnesium Oxide (MgO) for tunneling magnetoresistance (TMR) measurement in magnetic tunnel junction (MTJ) structures (see Ref. 18). The M2 layer is a synthetic antiferromagnetic (SAF) structure (see Ref. 19) and is permanently magnetized along one of the two orientations along its easy axis, say the $-z$-axis. The output of the gate is extracted from the MR measurement of the MTJ structure (layers M1 and M2 separated by the spacer) by passing a current I_{read}. The *Set* terminal is required to set the magnetization direction of the M1 layer opposite to that of the M2 layer.

Figures 2(a) and 2(b) show the potential profiles of the magnetostrictive nanomagnet (layer M1 in the Fig. 1) for different input vector combinations corresponding to NOR and NAND logic operations, respectively. The plots depict that the potential landscapes of the magnetostrictive nanomagnets can be inverted with application of voltages at the terminals A and B generating stress-anisotropy[5,25] in the nanomagnet, so that the minimum energy position changes from nanomagnet's easy-axis $(\theta = 0^\circ$ or $180^\circ)$ to its hard-axis $(\theta = 90^\circ)$. The output *logic 0* actually corresponds to some finite voltage due to small but non-zero resistance of the MTJ, however, such small voltages are not enough to invert the barrier and enable switching.

The potential profiles are shown when magnetization lies on its plane; however, consideration of magnetization's dynamics in full three-dimensional space is required for a complete 180° switching of magnetization even in the presence of room-temperature thermal fluctuations.[26] Computing methodologies utilizing such 180° switching mechanism between the two stable states of a shape-anisotropic magnetostrictive nanomagnet have not been proposed so far. Note that the potential energies of the corresponding nanomagnets for the NOR and NAND gates are drawn in their respective normalized scales. The shape-anisotropic energy barriers ($A = 0$, $B = 0$ cases) for both the NOR and NAND gates are of same magnitude since it is a design criterion that determines the thermal stability or the error-probability due to spontaneous switching of magnetization. The nanomagnets designed for the NOR and NAND gates need to be of same thickness should both types of the gates are required on a chip simultaneously.[27] Both of these universal logic gates can operate using nanomagnets with the same material and voltage level provided they are designed with different lateral dimensions (to be described later). The principles of operation of these two gates are shown in Fig. 3. Basically, during LOGIC operation, depending on the stress level and the type of gate, the potential barrier of the nanomagnet M1 gets inverted and the magnetization switches, which makes the magnetoresistance *low* and thus it performs the respective logic operation for the gates.

The design of the nanomagnets for devising NOR and NAND gates is different due to their respective logic operations. This can be understood from the modifications of the potential energy barriers required for the gates as depicted in Fig. 2. The critical stress needed to overcome the unperturbed shape-anisotropic potential barrier ($A = 0$, $B = 0$ case) is lower for the NOR gate than that of the NAND gate. The stress-anisotropy in a magnetostrictive nanomagnet is proportional to the product of stress and volume of the nanomagnet;[5,25] hence the volume of the nanomagnet for devising the NOR gate is required to be higher than the one used for the NAND gate. Now, the shape-anisotropy energy barrier height is proportional to a nanomagnet's volume and the degree of aspect ratio of the nanomagnet's elliptical cross-section for a given thickness.[5,25] Since the nanomagnet for devising the NAND gate is of lower volume, the aspect ratio of its elliptical cross-section needs to be higher. Thus, for a given thickness, the lateral dimensions of the nanomagnet for devising the NAND gate is smaller than the one for the case of the NOR gate.[28]

We have solved stochastic Landau-Lifshitz-Gilbert (LLG) equation[29–31] to design the universal logic gates NOR

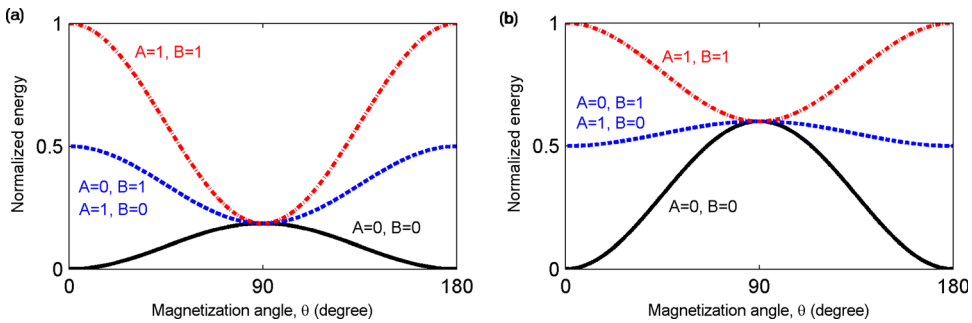

FIG. 2. Potential landscapes of the magnetostrictive nanomagnet (M1 layer) with different input vector combinations as a function of the angle θ subtended by its magnetization vector with the $+z$-axis for NOR and NAND logic operations, respectively. The potential profiles are shown when the magnetization vector lies on the magnet's plane, i.e., y–z plane. When no voltage is applied to either of the inputs A and B, the potential landscape is the shape-anisotropic energy barrier of the nanomagnet. (a) Potential landscapes corresponding to the NOR gate. When voltage is applied to either one of the inputs or both, the generated stress-anisotropy inverts the potential landscape and switching takes place. (b) Potential landscapes corresponding to the NAND gate. In this case, only when voltages are applied to both the inputs, the generated stress-anisotropy can invert the potential landscape and switching can take place.

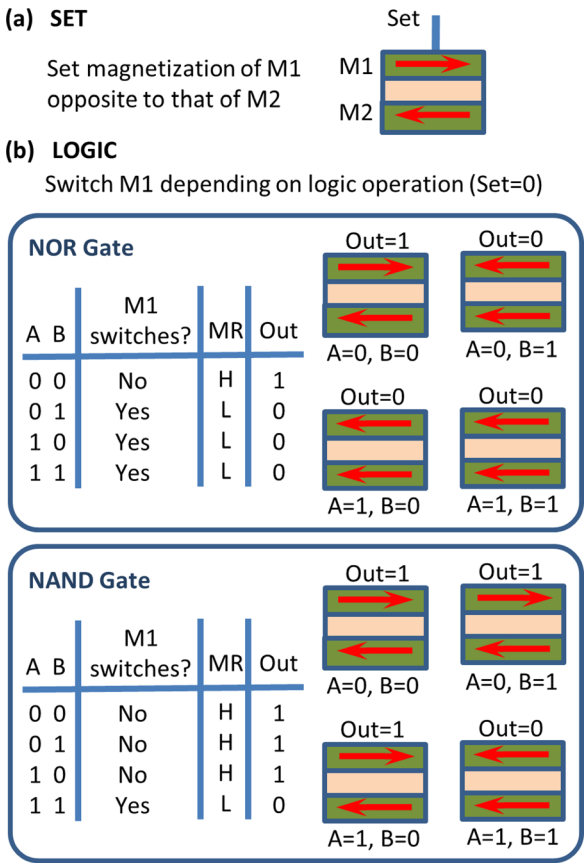

FIG. 3. Operations of straintronic universal logic gates. MR is *low* (L) [*high* (H)] depending on the parallel [anti-parallel] orientation of the magnetizations in the layers M1 and M2. (a) The SET operation switches the magnetization of the M1 layer to the opposite to that of the M2 layer. This operation should precede the LOGIC write operation in the M1 layer. (b) LOGIC operations of the universal logic gates NOR and NAND after the SET operation.

and NAND in the presence of room-temperature thermal fluctuations.[6] The material parameters that characterize the magnetostrictive layer made of polycrystalline Terfenol-D (TbDyFe) are as follows – Young's modulus (Y): 80 GPa, Magnetostrictive coefficient $((3/2)\lambda_s)$: $+90 \times 10^{-5}$, saturation magnetization (M_s): 8×10^5 A/m, and Gilbert's damping parameter (α): 0.1 (Refs. 6, 32–34). We model the nanomagnets as elliptical cylinders and the dimensions of the nanomagnets for designing the NOR and NAND gates are chosen as $117\,\text{nm} \times 102\,\text{nm} \times 6\,\text{nm}$ and $70\,\text{nm} \times 52\,\text{nm} \times 6\,\text{nm}$, respectively. These dimensions ensure that the nanomagnets have a *single* ferromagnetic domain.[28,35] Along with the material parameters, the dimensions ensure that the in-plane static shape-anisotropy energy barrier height is $\sim 60\,kT$ at room-temperature for both the gates. For the piezoelectric layer, we use lead-zirconate-titanate (PZT). We will assume that the maximum strain that can be generated in the PZT layer is 500 ppm,[36] which would require a voltage of 66.7 mV because $d_{31} = 1.8 \times 10^{-10}$ m/V for PZT[6] and the PZT layer is assumed to be 24 nm thick.[6] The corresponding stress is the product of the generated strain (500×10^{-6}) and the Young's modulus of the magnetostrictive layer. So the maximum stress that can be generated on the Terfenol-D layer is 40 MPa.

Switching delay and total energy dissipation are calculated following the prescription in Refs. 6 and 37. We determine the initial distributions of polar angle θ and azimuthal angle ϕ at room-temperature[38] and we perform a moderately large number (10 000) of simulations for each value of stress and gate type to generate the simulation results in this Letter. The ramp duration of stress is assumed to be 60 ps.[6] We assume that each of the inputs A and B to the logic gate can generate 15 MPa stress (corresponding to voltage 25 mv) on the magnetostrictive nanomagnet so that when both the inputs are turned ON, the total stress on the nanomagnet would be 30 MPa.

The read current I_{read} needs to be calculated in a way such that a gate upon concatenation to a subsequent stage can apply the same voltage of 25 mv at one input. We can determine and calibrate the MTJ resistance for both anti-parallel (R_{AP}) and parallel (R_P) conditions. Then we need to apply the following equation: $25\,mv = I_{read} \times R_{AP}$. With $R_{AP} = 25\,M\Omega$, the read current $I_{read} = 1\,nA$. Assuming $R_{AP} = 10\,R_P$,[39] we will have only 5 mV of voltages applied when both the inputs are *logic 0*; this corresponds to 3 MPa of stress on the magnetostrictive nanomagnet, which is not sufficient to switch its magnetization. Note that the application of a voltage at the *Set* terminal to switch the magnetization of M1 layer to the opposite to that of the M2 layer would require the knowledgebase of the magnetoresistance of the MTJ. If the relative orientation is anti-parallel, no voltage is applied; otherwise, a voltage is applied to switch the magnetization of the M1 layer to make the relative orientation anti-parallel.

Figures 4(a) and 4(b) show the distributions of switching delay and energy dissipation, respectively, for the NOR logic gate upon application of 15 MPa stress (only one input is ON), while Figs. 4(c) and 4(d) show the same for 30 MPa stress (when both inputs are ON). The mean energy dissipation to perform switching in a NOR LOGIC operation is less than 1.25 aJ at sub-nanosecond switching delay. Figures 4(c) and 4(d) show the distributions of switching delay and energy dissipation, respectively, for the NAND logic gate when both the inputs are ON (30 MPa stress). Note that when only one input is ON, it is not sufficient for switching to take place. For switching in a NAND LOGIC operation, the mean energy dissipation is around 0.35 aJ at room-temperature and the switching takes place in sub-nanosecond time-frame too. The overall mean energy dissipation can be much less if we consider switching for different input vector combinations, e.g., for NAND LOGIC operation, since switching of magnetization takes place only for one input combination ($A = 1$, $B = 1$), considering equal probability of different input vectors, the mean energy dissipation can be as low as 0.1 aJ at room-temperature. The SET operation also incurs similar amount of energy dissipation as of LOGIC operation when magnetization direction is required to switch. Note that with a pipeline of subsequent SET and LOGIC operations, the effective switching period is not affected. Such ultra-low-energy magnetic logic systems can be powered by energy harvesting assemblies[5,40–42] that can harvest energy from the environment without the need of an external battery. The SET operation precedes the LOGIC operation since after LOGIC operation the anti-parallel orientation between the magnetic layers may become parallel. However, it should be noted particularly for NAND LOGIC operation,

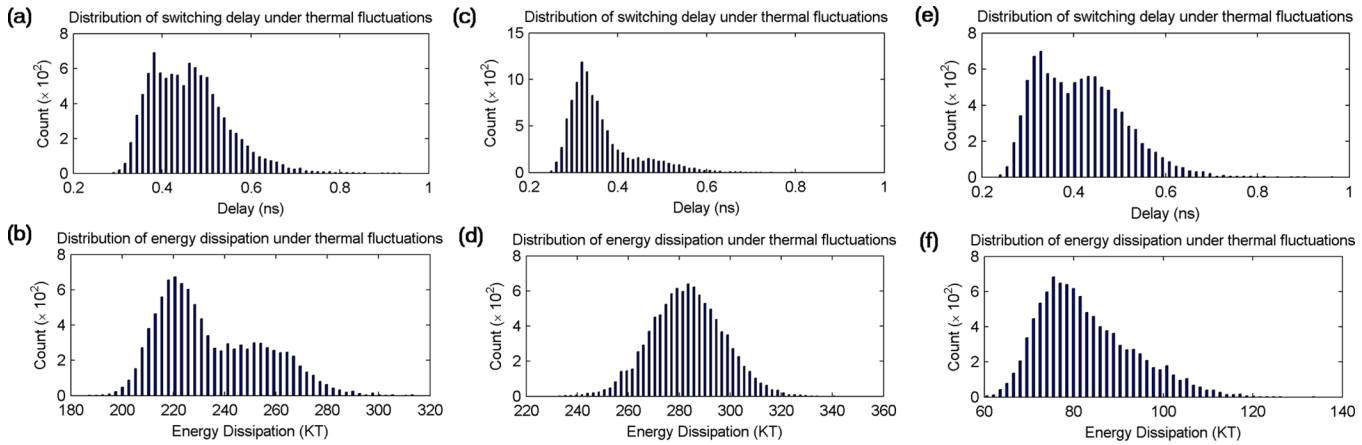

FIG. 4. Delay and energy distributions for switching of magnetization for the NOR and NAND gates at room temperature (300 K). (a) Distribution of the switching delay (with mean 0.46 ns and standard deviation 85 ps). (b) Distribution of energy dissipation (with mean 234.8 *kT* and standard deviation 20.5 *kT*) when only one input is ON (15 MPa stress) for the NOR gate. (c) Distribution of the switching delay (with mean 0.36 ns and standard deviation 72 ps). (d) Distribution of energy dissipation (with mean 283.2 *kT* and standard deviation 14.1 *kT*) when both the inputs are ON (30 MPa stress) for the NOR gate. (e) Distribution of the switching delay (with mean 0.41 ns and standard deviation 93 ps). (f) Distribution of energy dissipation (with mean 82.8 *kT* and standard deviation 10.5 *kT*) when both the inputs are ON (30 MPa stress) for the NAND gate.

the magnetic orientation may become parallel only if both the inputs are *logic 1*, while for the other three input combinations, the magnetic orientation between the layers remains anti-parallel, which does not necessitate any SET operation. System-level power-aware design methodologies can exploit this understanding to bypass any unnecessary SET operations.[43] For NOR logic, such advantage is marginal.

It needs to be emphasized that the inputs and output of the proposed straintronic logic gates are electrical in nature and hence there is no spin-to-charge conversion issue. Universal logic gates can be concatenated to perform any Boolean logic operation so any logic functionality can be implemented. However, unprecedented use of connectivity between the 2-input universal logic gates is not recommended, e.g., a majority logic gate or a 3-input logic gate may be required for different purposes in digital integrated circuits,[44] which can be implemented following the same methodology of using a *single* multiferroic element.

In conclusion, we have devised a logic design concept utilizing *single* multiferroic composites for the purposes of room-temperature computing that can be so energy-efficient that it can be powered from energy harvested from the environment. The basic building blocks are fast in operation, non-volatile (that can lead to instant turn-on computer), and they portend highly dense logical functionality per unit area because of using *single* multiferroic elements as universal logic gates. The proposed methodology is verified with a widely accepted model and it is within the reach of experimental implementation. Processors based on this paradigm can harbinger unprecedented applications such as medically implanted devices monitoring epileptic patient's brain to warn an impending seizure by drawing energy solely from the patient's body movements, or even energy radiated by wireless networks and television stations.

[1]S. A. Wolf, D. D. Awschalom, R. A. Buhrman, J. M. Daughton, S. V. Molnar, M. L. Roukes, A. Y. Chtchelkanova, and D. M. Treger, Science **294**, 1488 (2001).
[2]G. A. Prinz, Science **282**, 1660 (1998).
[3]S. A. Wolf, J. Lu, M. R. Stan, E. Chen, and D. M. Treger, Proc. IEEE **98**, 2155 (2010).
[4]W. Eerenstein, N. D. Mathur, and J. F. Scott, Nature **442**, 759 (2006).
[5]K. Roy, S. Bandyopadhyay, and J. Atulasimha, Appl. Phys. Lett. **99**, 063108 (2011).
[6]K. Roy, S. Bandyopadhyay, and J. Atulasimha, J. Appl. Phys. **112**, 023914 (2012).
[7]K. Roy, SPIN **3**, 1330003 (2013).
[8]G. E. Moore, Proc. IEEE **86**, 82 (1998).
[9]J. S. Kilby, *Nobel Lecture in Physics* (The Nobel Foundation, Sweden, 2000).
[10]S. Borkar, IEEE Micro. **19**, 23 (1999).
[11]T. Wu, A. Bur, K. Wong, P. Zhao, C. S. Lynch, P. K. Amiri, K. L. Wang, and G. P. Carman, Appl. Phys. Lett. **98**, 262504 (2011).
[12]N. Tiercelin, Y. Dusch, A. Klimov, S. Giordano, V. Preobrazhensky, and P. Pernod, Appl. Phys. Lett. **99**, 192507 (2011).
[13]H. K. D. Kim, L. T. Schelhas, S. Keller, J. L. Hockel, S. H. Tolbert, and G. P. Carman, Nano Lett. **13**, 884 (2013).
[14]N. Lei, T. Devolder, G. Agnus, P. Aubert, L. Daniel, J. Kim, W. Zhao, T. Trypiniotis, R. P. Cowburn, L. Daniel, D. Ravelosona, and P. Lecoeur, Nature Commun. **4**, 1378 (2013).
[15]R. P. Cowburn and M. E. Welland, Science **287**, 1466 (2000).
[16]J. Atulasimha and S. Bandyopadhyay, Appl. Phys. Lett. **97**, 173105 (2010).
[17]M. S. Fashami, K. Roy, J. Atulasimha, and S. Bandyopadhyay, Nanotechnology **22**, 155201 (2011).
[18]S. S. P. Parkin, C. Kaiser, A. Panchula, P. M. Rice, B. Hughes, M. G. Samant, and S. H. Yang, Nature Mater. **3**, 862 (2004).
[19]W. J. Gallagher and S. S. P. Parkin, IBM J. Res. Dev. **50**, 5 (2006).
[20]S. Mark, P. Durrenfeld, K. Pappert, L. Ebel, K. Brunner, C. Gould, and L. W. Molenkamp, Phys. Rev. Lett. **106**, 57204 (2011).
[21]B. Behin-Aein, D. Datta, S. Salahuddin, and S. Datta, Nature Nanotechnol. **5**, 266 (2010).
[22]P. Xu, K. Xia, C. Gu, L. Tang, H. Yang, and J. Li, Nature Nanotechnol. **3**, 97 (2008).
[23]H. Dery, P. Dalal, L. Cywinski, and L. J. Sham, Nature **447**, 573 (2007).
[24]A. Ney, C. Pampuch, R. H. Koch, and K. H. Ploog, Nature **425**, 485 (2003).
[25]S. Chikazumi, *Physics of Ferromagnetism* (Oxford University Press, USA, 1997).
[26]K. Roy, S. Bandyopadhyay, and J. Atulasimha, Sci. Rep. **3**, 3038 (2013).
[27]*Scanning Microscopy for Nanotechnology: Techniques and Applications*, edited by W. Zhou and Z. L. Wang (Springer, 2007).
[28]M. Beleggia, M. D. Graef, Y. T. Millev, D. A. Goode, and G. E. Rowlands, J. Phys. D: Appl. Phys. **38**, 3333 (2005).
[29]L. Landau and E. Lifshitz, Phys. Z. Sowjetunion **8**, 101 (1935).
[30]T. L. Gilbert, IEEE Trans. Magn. **40**, 3443 (2004).
[31]W. F. Brown, Phys. Rev. **130**, 1677 (1963).
[32]R. Abbundi and A. E. Clark, IEEE Trans. Magn. **13**, 1519 (1977).
[33]K. Ried, M. Schnell, F. Schatz, M. Hirscher, B. Ludescher, W. Sigle, and H. Kronmüller, Phys. Status Solidi A **167**, 195 (1998).
[34]R. Kellogg and A. Flatau, J. Intell. Mater. Syst. Struct. **19**, 583 (2008).

[35]R. P. Cowburn, D. K. Koltsov, A. O. Adeyeye, M. E. Welland, and D. M. Tricker, Phys. Rev. Lett. **83**, 1042 (1999).
[36]M. Lisca, L. Pintilie, M. Alexe, and C. M. Teodorescu, Appl. Surf. Sci. **252**, 4549 (2006).
[37]K. Roy, S. Bandyopadhyay, and J. Atulasimha, Phys. Rev. B **83**, 224412 (2011).
[38]See supplementary material at http://dx.doi.org/10.1063/1.4826688 for additional simulation results.
[39]T. Graf, S. S. P. Parkin, and C. Felser, IEEE Trans. Magn. **47**, 367 (2011).
[40]S. Roundy, "Energy Scavenging for Wireless Sensor Nodes with a Focus on Vibration to Electricity Conversion," Ph.D. dissertation (Mechanical Engineering, UC-Berkeley, 2003).
[41]S. R. Anton and H. A. Sodano, Smart Mater. Struct. **16**, R1 (2007).
[42]B. G. Karthik, S. Shivaraman, and V. Aditya, in *2011 IEEE Global Humanitarian Technology Conference (GHTC)* (IEEE, 2011), pp. 398–401.
[43]*Power Aware Design Methodologies*, edited by M. Pedram and J. M. Rabaey (Kluwer Academic Publishers, 2002).
[44]J. M. Rabaey, A. P. Chandrakasan, and B. Nikoliç, *Digital Integrated Circuits* (Pearson Education, 2003).