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# Reexamination of some spintronic field-effect device concepts

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Current interest in spintronics is largely motivated by a belief that spin-based devices (e.g., spin field-effect transistors) will be faster and consume less power than their electronic counterparts. Here we show that this is generally untrue. Unless materials with extremely strong spin-orbit interaction can be developed, the spintronic devices will not measure up to their electronic cousins. We also show that some recently proposed modifications of the original spin field-effect transistor concept of Datta and Das [Appl. Phys. Lett. **56**, 665 (1990)] actually lead to worse performance than the original construct. © *2004 American Institute of Physics*. [DOI: 10.1063/1.1784042]

A spate of device proposals have appeared over the last decade articulating spin-based analogs of conventional field-effect or bipolar junction transistors. The field-effect variety is motivated by a seminal concept due to Datta and Das,[1] who proposed an electronic analog of the electro-optic modulator. The Datta–Das device consists of a quasi-one-dimensional semiconductor channel with ferromagnetic source and drain contacts (Fig. 1). Electrons are injected with a definite spin orientation from the source, which is then controllably precessed in the channel with a gate-controlled Rashba spin-orbit interaction,[2] and finally sensed at the drain. At the drain end, the electron's transmission probability depends on the relative alignment of its spin with the drain's (fixed) magnetization. By controlling the angle of spin precession in the channel with a gate voltage, one can control the relative spin alignment at the drain end, and hence control the source-to-drain current. This realizes the basic "transistor" action. Because of this attribute, the Datta–Das device came to be known as the Spin Field-Effect Transistor (SPINFET) even though its original inventors aptly termed it an analog of the electro-optic modulator (not a "transistor").

There are many incarnations of the SPINFET (see, e.g., Refs. 3–5). All of them however rely on the basic concept of modulating the transistor's source-to-drain current by varying the Rashba interaction in the channel with a gate voltage. Therefore, the present analysis is perfectly general and applies to all of them. We show that in terms of common performance metrics (power dissipation, transconductance, unity gain frequency, etc.), the performance projections for a SPINFET are below those for a conventional silicon or GaAs field-effect transistor.

The following analysis applies to a SPINFET with a strictly one-dimensional (1D) channel. The 1D SPINFET is the ideal device with the best possible performance for two very important reasons. The first reason was identified in Ref. 1 itself; one-dimensional carrier confinement eliminates the angular spread in the electron's wave vector, which results in the strongest conductance modulation. In fact, only in a strictly 1D channel can the "off" conductance of the device fall to zero resulting in no leakage current in the off state. This is extremely important to avoid standby power dissipation if two SPINFETs, one biased in the positive transconductance region and another in the negative transconductance region, are connected in series to act like a complementary metal oxide semiconductor field-effect transistor (CMOS). The present dominance of CMOS in virtually all electronic circuits is due to the property that there is no standby power dissipation because the leakage current in a conventional MOS transistor is virtually zero when it is turned off. Therefore, at the very outset, it is obvious that only a 1D SPINFET can have any chance of competing with present day silicon CMOS devices. The second reason to prefer a strictly 1D channel is that the major spin relaxation mechanism in the channel (D'yakonov-Perel') can be completely eliminated if transport is single channeled.[6] Therefore, a 1D channel is always optimum.

The maximum conductance of a strictly 1D channel is $2e^2/h$. Since the drain current in a ballistic 1D channel will saturate when the source-to-drain bias $V_{SD}$ becomes equal to

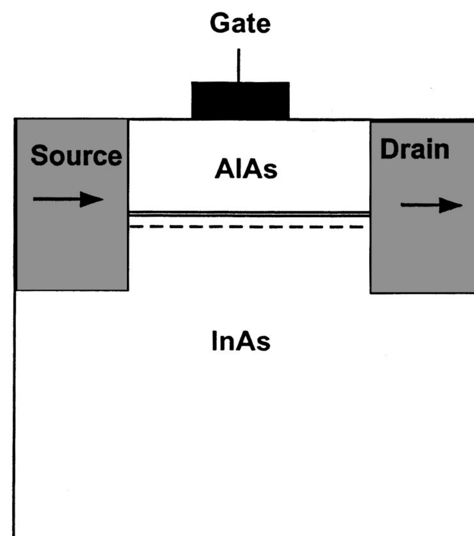


FIG. 1. Schematic of a Spin Field-Effect Transistor after Ref. 1.

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$E_F/e$ ($E_F$ is the Fermi energy in the channel), we have

$$I_D|_{\rm sat}=2eE_F/h. \quad (1)$$

The switching voltage $V_{\rm th}$ to turn the SPINFET from the "on" state to the "off" state is the gate voltage required to precess the spin in the channel through an angle of $\pi$ radians. Using the result of Ref. 1, this voltage is

$$V_{\rm th}|_{\rm SPINFET}\approx \hbar^2\pi/(2m^*L\zeta), \quad (2)$$

where $m^*$ is the effective mass of the carrier in the channel, $L$ is the channel length, and $\zeta$ is a proportionality constant that describes the gate voltage dependence of the Rashba coupling constant $\eta$. We can theoretically estimate $\zeta$. According to Refs. 7 and 8,

$$\eta=\frac{\hbar^2}{2m^*}\frac{\Delta(2E_g+\Delta)}{E_g(E_g+\Delta)(3E_g+2\Delta)}\frac{2\pi e^2N_s}{\kappa}, \quad (3)$$

where $e$ is the electronic charge, $E_g$ is the band gap, $\Delta$ is the spin-orbit splitting in the valence band, $\kappa$ is the static dielectric constant, and $N_s$ is the surface electron concentration at the interface of the channel ($N_s$ is related to the interfacial electric field in the channel inducing a structural inversion asymmetry and the Rashba effect). From standard MOS theory, $eN_s=(\kappa/d)(V_G-V_T)$, where $d$ is the thickness of the gate insulator, $V_G$ is the gate voltage, and $V_T$ is the threshold voltage to induce an inversion layer charge in the channel. Using this result in Eq. (3), we find that

$$\zeta=\frac{\partial\eta}{\partial V_G}=\frac{\hbar^2}{2m^*}\frac{\Delta(2E_g+\Delta)}{E_g(E_g+\Delta)(3E_g+2\Delta)}\frac{2\pi e}{d}. \quad (4)$$

We will assume an InAs channel and use material parameters from Ref. 9. To compare with experiment,[10] we will assume that $d=20$ nm. This yields the theoretical value of $\zeta=5\times 10^{-29}$ C m. Equation (4) predicts a linear dependence of $\eta$ on the gate voltage $V_G$. Experimentally, one finds the same *linear* dependence,[10] and the experimentally observed value of $\zeta\approx 8\times 10^{-31}$ C m.[10] The theoretical value is about 60 times larger than the experimental value, indicating that further experiments are required.

We will now compare the switching voltage of a 1D SPINFET with that of a traditional 1D MOSFET. At low temperatures, the switching voltage of a traditional ideal MOSFET (the voltage required to deplete the channel of all carriers) is $E_F/e$. Therefore,

$$\frac{V_{\rm th}|_{\rm SPINFET}}{V_{\rm th}|_{\rm MOSFET}}\approx\frac{\hbar^2\pi e}{(2m^*L\zeta E_F)}. \quad (5)$$

In order to maintain single subband occupation, we will assume that $E_F$ is less than the energy separation between subbands, which is about 3 meV in InAs 1D channels.[8] Then, the SPINFET will have a lower switching voltage than a traditional FET *only if* its channel length $L>4.88$ $\mu$m. In calculating this, we assumed the theoretical value of $\zeta$. If we had assumed the experimental value instead, $L$ has to be larger than 293 $\mu$m!. Therefore, it is obvious that for any submicron channel length (let alone nanoscale devices), the SPINFET will have a much higher switching voltage than a traditional MOSFET. This immediately shows that the SPINFET is *not a lower* power device. (the dynamic power dissipated during switching a transistor is proportional to the square of the switching voltage).

It is of course obvious that we can decrease the switching voltage of a SPINFET by decreasing the gate insulator thickness $d$. In $Si/SiO_2$ technology, gate insulator thicknesses approaching 1 nm is possible without causing significant gate leakage, but that may not be possible in systems such as AlAs/InAs (where the lower gap semiconductor is chosen for strong Rashba coupling) because the barrier height between the semiconductor and insulator is not nearly as high. We may be limited to a gate insulator thickness of 5 nm or larger in the AlAs/InAs system, which still makes the switching voltage of a submicron SPINFET larger than that of a submicron MOSFET. Reducing the gate insulator thickness also has deleterious effects on the unity gain frequency since it increases the gate capacitance [see Eq. (7) later].

Next, we consider the transconductance of a SPINFET. This is an important parameter since it determines device amplification, as well as bandwith or, equivalently, device speed. The transconductance of the SPINFET is

$$g_m\approx I_D|_{\rm sat}/V_{\rm th}=2eE_Fm^*L\zeta/(\pi^2\hbar^3), \quad (6)$$

where we have assumed that $V_{\rm th}$ is small enough that $E_F$ does not vary significantly as the gate voltage swings over an amplitude of $V_{\rm th}$. Equation (6) yields $g_m=6.5\times 10^{-6}L$ S (where $L$ is the channel length expressed in microns). It is actually more meaningful to calculate the transconductance per unit channel width since in conventional MOSFETs, the transconductance is proportional to the channel width. For a 1D channel, we will assume that the confinement potential along the width is parabolic, so that the effective width of the channel is given by $W_{\rm eff}=\sqrt{\hbar/(2m^*\omega)}$.[11] Since $\hbar\omega=3$ meV, $W_{\rm eff}=22$ nm. Therefore, the transconductance per unit channel width is $295L$ mS/mm, where, once again, $L$ is expressed in microns. For submicron channel lengths, $g_m<295$ mS/mm, which is considerably less than what is achieved with GaAs high electron mobility transistors.

The unity gain frequency $f_T\leqslant g_m/C_g$, where $C_g$ is the gate capacitance given by $C_g=\kappa_i\epsilon_0LW_{\rm eff}/d$ ($\kappa_i$ is the relative dielectric constant of the gate insulator). Accordingly,

$$f_T\leqslant 2eE_Fm^*d\zeta/(2\pi^3\kappa_i\epsilon_0\hbar^3W_{\rm eff}). \quad (7)$$

We will assume that the gate insulator is AlAs (relative dielectric constant $\kappa_i\approx 8.9$[12]) and that $d=20$ nm, as before. Using these values in Eq. (7), we find that $f_T\leqslant 30$ GHz. This is less than what has already been demonstrated for GaAs MESFETs.[13]

We will conclude this letter by examining two recently proposed modified versions of the SPINFET that claimed to provide better performance than the original proposal of Ref. 1. The first version[3] purports to replace a strictly 1D channel, where only the lowest subband is occupied, with a *quasi 1D* channel where *two* subbands are occupied, in order to provide better spin control. We find this to be completely counterproductive for many reasons. First, multichanneled transport (where two subbands are occupied) will not eliminate D'yakonov–Perel' spin relaxation; that can happen only in strictly single channeled transport.[6] Therefore, a two-subband device is more vulnerable to spin flip scattering. Second, the presence of two occupied subbands can result in spin-mixing effects[14] that are harmful for the SPINFET. Third, multiple gates are required in the proposal of Ref. 3 for conductance modulation, and these gates have to be synchronized precisely in order to turn the device off. This is an

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additional engineering challenge that was not required in the original proposal of Ref. 1.

Another type of SPINFET that claims to be able to release the requirement of ballistic transport, which is necessary in the original Datta-Das device has recently been proposed.[4] The idea here is to balance the Rashba interaction[2] with the Dresselhaus interaction[15] (using a gate to tune the Rashba interaction). When they are exactly balanced, the eigenspinors in the channel are $[1,\pm\exp(i\pi/4)]$ which are spins polarized on the $x-y$ plane subtending an angle of $\pi/4$ with the $x$ or $y$ axis. In the convention of Miller indices, we call this axis the [1 1 0] axis. Then, by using a ferromagnetic source contact that is magnetized in the [1 1 0] direction, one can inject all spins into one of the eigenstates. Such a spin will traverse the channel without flipping (unless there are magnetic scatterers) since it is an eigenstate in the channel. However when the gate voltage is detuned to unbalance the Rashba and Dresselhaus interactions, the eigenspinors are no longer $[1,\pm\exp(i\pi/4)]$, but become wave-vector dependent. Therefore, any nonmagnetic scatterer (impurity, phonon, etc.) which changes the electron's wave vector, can also flip the spin. A spin injected in the [1 1 0] direction is no longer an eigenstate and will flip in the channel. The drain is also magnetized in the [1 1 0] direction, which will not transmit the flipped spin. Therefore, the device conductance will decrease. This device is "on" when the gate voltage exactly balances the Rashba and Dresselhaus interactions, and "off" otherwise.

It is difficult to calculate the off-conductance of this device since that depends on the frequency and nature of spin flip scatterings that occur when the Rashba and Dresselhaus interactions are unbalanced. However, it is obvious that the off-conductance is *not zero*. In fact, if the device is long enough, then a spin arriving at the drain contact is equally likely to be parallel or antiparallel to the drain's magnetization. Therefore, the minimum value of the off-conductance is one-half of the on-conductance. Such a device is not suitable as a transistor in digital applications (since the on- and off-states are not well separated) and even for analog applications, the device is less preferable to the original Datta Das proposal since the transconductance of this device will be roughly one-half of the transconductance of the Datta–Das device. Most important, this device has a large leakage current during the off-state (approximately one-half of the on-current). Therefore, such devices will lead to unacceptable standby power dissipation.

In conclusion, *present versions* of spin-based field-effect transistors are not likely to be competitive with their electronic counterparts. We have also shown that proposed improvements over the original Datta–Das device of Ref. 1 are actually counter-productive. It is therefore unlikely that present versions of spintronic field effect transistors will play a significant role in combational digital, analog or mixed signal circuits. However, they can certainly play a role in memory, where high gain, high frequency, etc. are not necessary. Spintronic devices may also have better noise margin since spin does not easily couple to stray electric fields (unless the host material has very strong spin-orbit interactions). It is also possible that spintronics may be able to outpace electronics in nonconventional applications such as single spin logic,[16–18] spin neurons,[19] and using spin in a quantum dot to encode qubits.[20–23]


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