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A. Varfolomeev
Kurchatov Institute

D. Zaretsky
Kurchatov Institute

V. Pokalyakin
Institute of Radio-Engineering and Electronics RAS

See next page for additional authors

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Admittance of CdS nanowires embedded in porous alumina template

A. Varfolomeev and D. Zaretsky
Russian Research Center "Kurchatov Institute," Kurchatov sq. 1, Moscow, Russia

V. Pokalyakin and S. Tereshin
Institute of Radio-Engineering and Electronics RAS, Mohovaya st.11, Moscow, Russia

S. Pramanik and S. Bandyopadhyay
Department of Electrical and Computer Engineering, Virginia Commonwealth University, Richmond, Virginia 23284

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CdS nanowires of 10 nm diameter, electrodeposited in porous alumina films, had shown a conductance bistability in the past [Appl. Phys. Lett. **76**, 460 (2000)]. The conductance has a high (ON) and a low (OFF) state. In the ON state, different sets of nanowires display qualitatively different relation between the conductance and capacitance. We propose a model to explain this anomalous behavior. Based on this model, we predict that the inelastic mean free path of electrons in the nanowires is 3–3.5 nm at room temperature. This short mean free path may be a consequence of acoustic phonon confinement. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2185729]

CdS nanowires, synthesized by electrodepositing CdS in 10-nm-diam pores of an anodic alumina film, show a conductance bistability. The conductance switches reproducibly between a low (OFF) and a high (ON) state upon the application of a suitable voltage bias across the length of the nanowires.[1] The two states are nonvolatile (lifetime >1 year) and their conductances differ in magnitude by four orders, so that this effect has potential applications in high density nanowire static random access memory. Recently, a phenomenological model was proposed to explain the origin of this bistability.[2]

In this letter, we report an anomalous behavior observed in the admittance of the nanowires when they are in the high-conductance (ON) state. Conductances and capacitances are measured between different (equal area) contact pads delineated on the same sample, so that we probe different sets of nanowires. The sets of nanowires exhibiting the largest capacitance per unit area ($C>0.04$ F/m^2) show the conductance increasing with decreasing capacitance, while the others ($C<0.04$ F/m^2) show the conductance decreasing with decreasing capacitance. A model is proposed to explain this behavior.

Nanowire samples of CdS in porous alumina were prepared by the method described in Ref. 1. The average length of the nanowires is 200 nm and the diameter is 10 nm. For electrical measurement, semitransparent Au contacts of area 0.6 mm$\times$0.6 mm were evaporated on the top through a mask. Since the wire density is $>10^{11}$/cm^2, more than 3.6×10^8 wires are covered by each contact pad. Admittance was measured by a standard *LCR* meter at a frequency of 1 MHz by connecting one terminal of the meter to a Au pad and the other terminal to the bottom Al foil as shown in Fig. 1. The meter measures the resistance and capacitance separately. There is no dc bias across the length of the nanowires.

In Fig. 2, we show the equilibrium energy band diagram along the length of the nanowire in the high-conductance state. This is adopted from Ref. 2. There is an accumulation layer of electrons at the interface between the CdS and the alumina barrier layer caused by filled electron traps that reside at this interface. They result in band bending that lowers the barrier to current flow and cause the high conductance state.[2] An applied ac bias can cause charge fluctuations in different regions of the nanowire, giving rise to different dominant capacitances, C_1, C_2 and C_3 shown in Fig. 2. The capacitance C_1 will have a value given by approximately $\varepsilon_{CdS}/d_{CdS}$ (per unit area) where ε_{CdS} is the permittivity of CdS and d_{CdS} is the unaccumulated length of the nanowire. Since the relative permittivity of CdS is 9 and $d_{CdS}\sim200$ nm, $C_1=4\times10^{-4}$ F/m^2 which is two orders of magnitude smaller than the largest capacitance we measure and a factor of 2 smaller than the smallest capacitance we measure. Therefore, C_1 is outside the range of measured capacitance; hence, it cannot be the relevant capacitance. Similarly, $C_3=\varepsilon_{alumina}/d_{alumina}$ where $\varepsilon_{alumina}$ is the permittivity and $d_{alumina}$ is the thickness of the barrier layer. Since $\varepsilon_{alumina}=4$ and $d_{alumina}=20$ nm,[3] $C_3=1.77\times10^{-3}$ F/m^2, which is 22 times smaller than the largest capacitance we measure, but two times larger than the smallest capacitance we measure. Therefore, C_3 may play a role in the nanowires displaying the smallest capacitances, but not in any other case. That leaves C_2 which will be given by $\varepsilon_{CdS}/d_{acc}$, where d_{acc} is the width of the accumulation layer. Since the measured capacitance per unit area varied from 5.3×10^{-2} to 8×10^{-4} F/m^2, the range of d_{acc} is between 1.5 and 100 nm. This range is typical of accumulation layers formed in semiconductors.

In Fig. 3, we plot the measured resistance as a function of the effective width d where $d=\varepsilon_{CdS}/C_{measured}$. The differ-

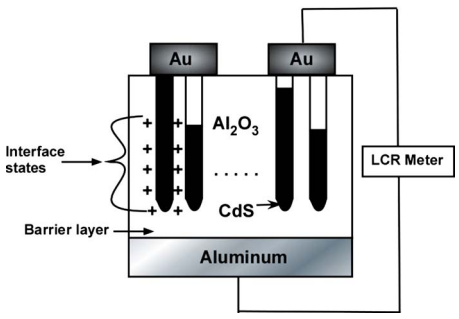

FIG. 1. Cross section of the sample structure and the measurement setup.

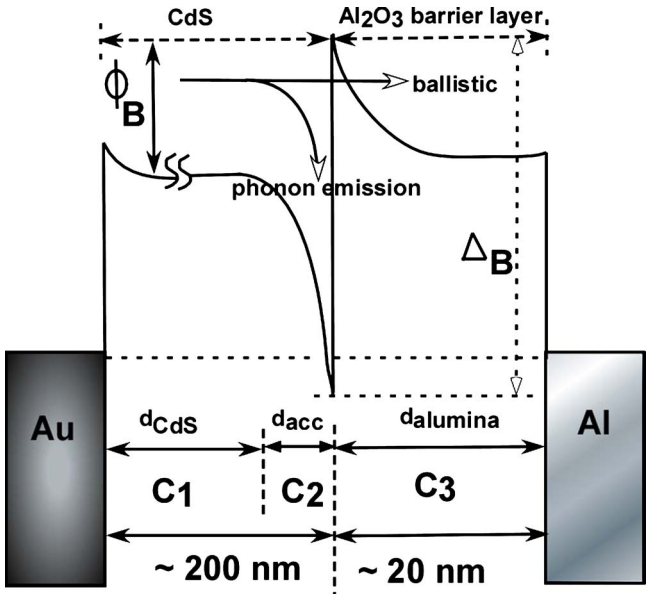

FIG. 2. Equilibrium energy band diagram of the nanowire in the high conductance state showing the widths of the different layers.

ent data points correspond to different sets of nanowires measured between different Au contact pads and the bottom aluminum. With the sole exception of the last two data points, $d < d_{\text{alumina}}$ and therefore d must correspond to the accumulation layer thickness d_{acc}.

We first note that if $d_{\text{acc}} < 3.5$ nm, then resistance R decreases with increasing d_{acc}. This is consistent with the model presented in Ref. 2. The accumulation layer pulls down the potential barrier caused by the alumina layer, which then increases the tunneling and thermionic emission currents, thereby causing the high conductance state. If there are more accumulation charges, corresponding to a larger d_{acc}, then the barrier will be pulled down more and the resistance should decrease. This is exactly what we see when $d_{\text{acc}} < 3.5$ nm, However, when $d_{\text{acc}} > 3.5$ nm, the behavior changes and resistance increases with increasing d_{acc}. This anomalous behavior can be explained in the following manner.

The transmission probability (and therefore the conductance) of electrons that traverse the accumulation region *without* suffering inelastic collisions are determined by the height of the potential barrier ϕ_B. However, those electrons that suffer inelastic collisions and emit phonons lose their kinetic energy and fall into the conduction band notch at the interface between CdS and alumina. For them, the potential barrier is much larger (Δ_B) and they cannot cross this potential barrier and contribute to current. Thus, the resistance of the structure increases with increasing probability of suffering an inelastic collision in the accumulation layer. This probability increases with increasing width of this layer, once the width exceeds the inelastic mean free path. Therefore, we expect to see an increase in resistance with increasing d_{acc} once d_{acc} exceeds the inelastic mean free path. Based on this premise, we estimate from the data in Fig. 3 that the inelastic mean free path of electrons in the CdS nanowires is about 3 nm at room temperature.

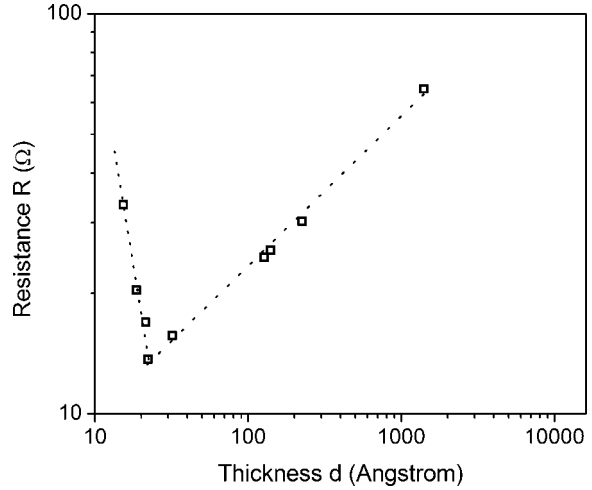

FIG. 3. Resistance vs effective accumulation layer width d measured for different sets of nanowires. The width $d = \varepsilon_{\text{CdS}}/C$ where C is the measured capacitance.

Finally, the question that remains to be answered is why d_{acc} varies so much from one set of nanowires to another. This quantity varies from 1.5 to about 100 nm. The variation comes about because the charge in the accumulation layer is caused by traps at the interface of CdS and alumina,[2] and the trap density can vary widely. As a result, it is entirely possible that the accumulation layer charge can also vary significantly. This charge density $n(x)$ inside the accumulation layer varies with position x according to[4]

$$n(x) = n_0 a^2/(a+x)^2, \tag{1}$$

where n_0 is the electron density at $x=0$ and a is the Debye (or Fermi–Thomas) screening length that depends on n_0. Therefore, the total accumulation charge per unit area is given by

$$Q_{\text{acc}} = -q\int_0^{d_{\text{acc}}} n(x)dx = -qn_0a^2\int_0^{d_{\text{acc}}} \frac{1}{(a+x)^2}dx$$
$$= -2qn_0a^2[1/(2a)^3 - 1/(2a+d_{\text{acc}})^3], \tag{2}$$

where q is the electronic charge.

Inverting the above relation, we find that d_{acc} increases *superlinearly* with Q_{acc}. Therefore, d_{acc} can vary significantly even for moderate changes in Q_{acc}, or equivalently moderate changes in the trap density.

We have also found that when $d < 3.5$ nm, the measured resistance $R \sim d^{2.2\pm0.22}$, whereas when $d > 3.5$ nm, $R \sim d^{0.37\pm0.01}$. These power dependences are currently being investigated further.

In conclusion, we have observed a nonmonotonic dependence of the resistance of nanowires on the capacitance, which we correlate to the width of the accumulation layer. Based on a model that we have proposed to explain this behavior, we predict that the inelastic mean free path in the nanowires is 3–3.5 nm at room temperature. This mean free path is surprisingly short. We speculate that this happens owing to possible acoustic phonon confinement in the nanowires, which have a diameter of 10 nm. Acoustic phonon confinement is known to increase the scattering rate due to electron-acoustic phonon interaction significantly,[5,6] thereby causing a short mean free path.

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